

The Solar Ultraviolet Imaging Telescope: detector characterization and readout electronics testing

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ABSTRACT

The *Solar Ultraviolet Imaging Telescope (SUIT)* is one of the payloads onboard the Aditya-L1 mission. It will perform full disc imaging of the Sun in the near-ultraviolet (UV) wavelength range of 200–400 nm. This provides near-simultaneous observations of the Sun from the photosphere and chromosphere. A back-illuminated, enhanced UV charge coupled device (CCD) of size 4096 (H) × 4136 (V) pixels, with a pixel size of 12 μm, is used as an imaging element in *SUIT*. The CCD characterization and the readout electronics development and testing were performed in-house at the Space Astronomy Group, U R Rao Satellite Centre, ISRO. The test set-up and procedures are explained and the measured values of various parameters including noise, dark current, gain, linearity, and cross-talk are presented in this paper. The results show a satisfactory performance from the CCD as well as the readout electronics to meet the specifications required by the *SUIT* payload.

Key words: Instrumentation – Aditya L1 – Camera sensor calibration – CCD – Detector electronics.

1 INTRODUCTION

The *Solar Ultraviolet Imaging Telescope (SUIT)* (Ghosh et al. 2016; Tripathi et al. 2017) is the second largest payload among the seven payloads onboard the upcoming space-based solar observatory Aditya-L1 (Seetha & Megala 2017; Tripathi et al. 2022). *SUIT* will be imaging the Sun in the near-ultraviolet (UV) wavelength range (200–400 nm) in 11 spectral bands using narrow as well as medium band pass spectral filters covering a field of view of ±1.5 R_⊙ with a plate scale of 0.7 per pixel. Fig. 1 shows the schematic diagram of the *SUIT* payload. A thermal filter is placed at the entrance baffle that will filter out the visible and infrared light and reduce the flux in UV. The transmission filter has an average transmission range of 0.1–0.45 per cent in 200–400 nm range and about 0.2 per cent in the visible band (Ghosh et al. 2022). So, in the operating wavelength of 200–400 nm, an average power of 15.6 mW (per nm) enters the instrument, and only a small fraction of this power, of about

3.9 μW, is transmitted by the filter. It is followed by primary and secondary mirrors that are placed off-axis with Ritchey–Chrétien configuration. The filter wheel assembly consists of two filter wheels with eight filter slots in each wheel. It has 11 science filters and five combination filters. Behind the filter wheels is the field-correcting mechanism consisting of a field-correcting lens mounted on a piezo motor. Flat fielding is done using a set of 16 Light Emitting Diodes (LEDs) (eight at 255 nm and eight at 355 nm), mounted to a circular panel after the focusing mechanism. The exposure control is done using a vane shutter fixed to a stepper motor. A charge coupled device (CCD) detector is placed at the focal plane.

SUIT uses a back-illuminated e2v CCD detector consisting of 4096 × 4136 pixels of size 12 microns each. This device is similar to the CCD used for the visible imager in the European Space Agency (ESA) *Euclid* mission (Cropper et al. 2012) and ESA qualifications apply to this device. The image sensor is divided into two image areas A and D (Fig. 2). These image areas can be read from one, two, or all four readout amplifiers in full-frame or binned mode by controlling the direction of transfer using clocks. The four-channel simultaneous readout reduces the readout time and hence is the default readout mode. The CCD contains 50 dark pixel columns on either side that will be used for understanding dark current properties. These dark pixels are present outside the imaging area and are unexposed. While clocking the CCD, the dark pixels are first obtained, followed by the

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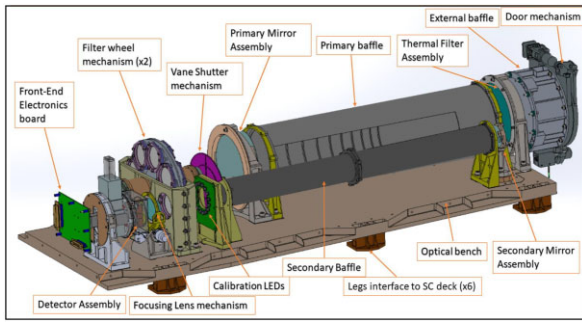


Figure 1 Schematic representation of the *SUIT* payload.

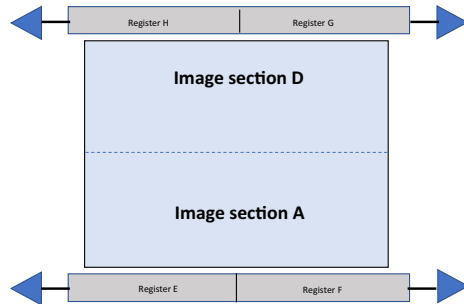


Figure 2 Figure shows the *SUIT* CCD imaging sensor. The image area consists of two sections and four readout channels.

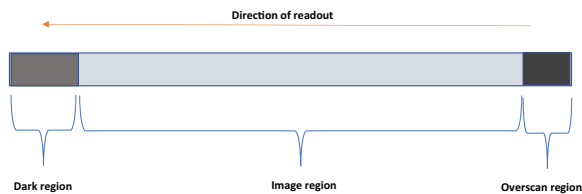


Figure 3 Figure shows dark, image, and overscan pixels in a row. Every row consists of dark pixels followed by image pixels. Overscan is obtained by clocking the CCD beyond the image region.

image pixels. Overscan pixels are obtained by clocking the CCD beyond the image region (Fig. 3). In the final image, the overscan and dark regions are displayed together on either side of the image region. The image can be visualized as four different quadrants, referred to as E, F, G, and H, each representing a region, readout through a different channel of a four-channel readout along with dark and overscan columns (see Fig. 4). The number of overscan columns can be 14 to 254. The CCD can be used to acquire a full-frame image, an image binned by 2×2 pixels, and a region of interest (RoI) image. The technical specifications for the CCD are summarized in Table 1.

The CCD operation is performed and controlled using a set of electronics referred to here as, the *SUIT* detector readout electronics. This electronics is also used to perform various payload operations. All these operations based on predefined operational modes require various control, monitoring, and processing tasks that are performed by four different modules in the *SUIT* readout electronics. They are:

- (i) Analogue electronics.
- (ii) Timing electronics.

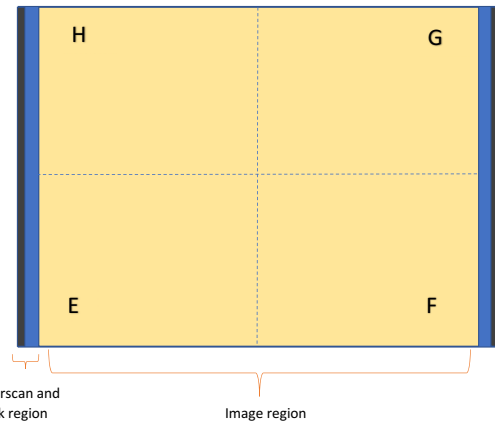


Figure 4 Figure shows the *SUIT* CCD image along with the dark and overscan regions. The image can be visualized as four different quadrants that are read using different readout channels E, F, G, and H.

Table 1. Technical specifications of *SUIT* CCD.

Parameter	Specifications
Array size	4096 (H) by 4136 (V)
Pixel size	12 μm
Full well capacity (pixel)	190k electrons
Full well capacity (register)	300k electrons
Number of outputs	4
Antiblooming	No
Operation mode	Non-inverted

- (iii) Processing electronics.
- (iv) Motor electronics.

The analogue electronics board consists of a clamp-and-sample-based correlated double sampling (CDS) circuit that samples the voltage in each pixel. It was employed to reduce the noise and offset in the analogue signal. CDS works by subtracting the offset voltage from the signal voltage which reduces the impact of various sources of noise, including thermal noise, read noise, and dark current there by improving the overall quality of the image. Offset is generated using a digital-to-analogue converter (DAC) and added to signals. Further amplification of signals is performed by a programmable gain amplifier circuit and amplified signals are fed to a 16-bit analogue-to-digital converter (ADC) for digitization. The ADC data are sent to processing electronics for further processing that is required for the payload operation.

The timing electronics board contains mainly a Field Programmable Gate Array (FPGA) based CCD clocks (line/pixel) and serial DAC-based programmable CCD bias generation circuits. The timing electronics board also consists of a DAC-based constant current LED driver circuit to drive 16 LEDs in the LED panel used for calibration (flat fielding).

The processing electronics board is used to perform various payload operations based on predefined operational modes. This board utilizes another FPGA and software written in C for Core 8051 to perform the on-board control and processing functions like generating a flare trigger from data received from other X-ray payloads onboard the Aditya L1 (Sankarasubramanian et al. 2017), localization of a flare using *SUIT* data, tracking the selected RoI, and adjusting exposure time depending on flare intensity. These functions are carried out using a set of program sequences stored in EEPROM and FPGA memory and the four images in SDRAM.

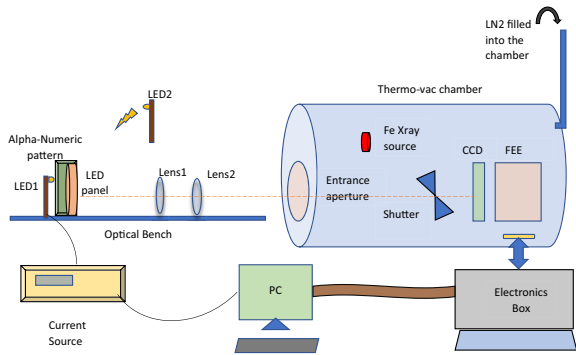


Figure 5 The test set-up used for the CCD characterization and testing of the readout electronics package.

The motor electronics board consists of driver electronics for the shutter motor used for exposure control and a piezo motor used for focus adjustment. It also consists of readout circuits for a resolver that specifies the position of the shutter motor and a linear optical encoder that gives the position of the piezo motor.

Apart from these four electronic boards, the front-end electronics board is placed along with the CCD and it performs the first stage of signal amplification. The *SUIT* electronics package is powered using two DC–DC converters placed in the bottom tray of the electronics package. The fully assembled *SUIT* electronics package was tested with Engineering Model (EM) /Qualification Model (QM) grade CCD to check the performance and functionalities. The test results presented in this paper correspond to those obtained using the QM CCD (which is equivalent to Flight Model (FM)) and FM readout electronics package.

The test set-up used for the testing is explained in Section 2. Sections 3–5 describe the results of the CCD characterization and readout electronic packages (analogue and timing) testing. The results are summarized in Section 6. The development of onboard processing algorithms and testing of processing electronics package is discussed in Varma et al. (2023). The working of the shutter and piezo motor along with motor electronics package testing is discussed in Anurag (in preparation).

2 TEST SET-UP

The test set-up shown in Fig. 5 was used to characterize the CCD and test the *SUIT* electronics package.

The CCD is placed inside a thermo-vac chamber and liquid nitrogen (LN2) is pumped to cool the CCD. The CCD temperature is continuously monitored and the LN2 flow rate is adjusted to keep the CCD temperature between -55 to -65°C . A mechanical vane controlled by a stepper motor is placed in front of the CCD for exposure control. Also, a ^{55}Fe X-ray source is placed in front of the CCD, away from the line of sight of the entrance aperture of the thermo-vac chamber. The X-ray source is used for gain and charge transfer efficiency (CTE) measurements. An alpha-numeric pattern printed on paper is placed in front of the CCD and is imaged onto the CCD. An LED (LED1) is placed behind this paper and is connected to a current source. The LED1 is used to simulate a flare light curve intensity profile required for testing the flare localization algorithm in processing electronics. The flare light curve is simulated through LED1 by varying the input current through a current source (for details see Varma et al. 2023). The current profile of the LED mimics a flare light curve (derived from *IRIS* Mg II h slit-jaw images) and as a result, the LED intensity simulates the flare light curve profile since

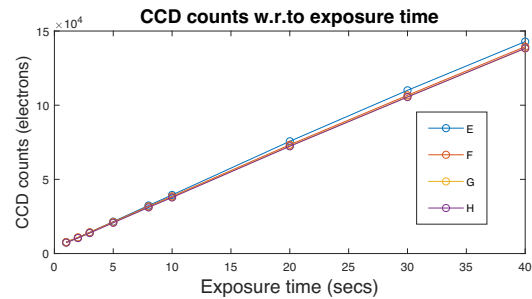


Figure 6 Mean CCD output intensity (for different channels) with respect to the exposure time for constant ambient light.

the LED intensity is linearly related to the input current. Another LED (LED2) is placed opposite to the paper (object) to illuminate it and the alpha-numeric pattern on the paper is imaged onto the CCD using a lens system. The lens system consists of two converging lenses, lens 1 (focal length 30 cm, aperture size 15 cm) and lens 2 (focal length 30 cm, aperture size 5 cm). Here, two lenses are used due to set-up limitations. The front end electronics package is placed behind the CCD inside the thermo-vac chamber. The *SUIT* electronics package is placed outside the thermo-vac chamber and is connected to the CCD via a harness. The LED panel is placed in front of the object plane during LED testing and is removed for the remaining tests. The commands used to run the tests are given through a computer which is also used to store and analyse the data.

3 DETECTOR CHARACTERIZATION

The *SUIT* design demands excellent values for various characteristic parameters of the CCD. It is required to have high CTE (greater than 99.9999 per cent), good linear response (non-linearity under 1 per cent), low dark current (less than 1 electron per pixel per second), and negligible cross talk (around 1 electron per 10 000 electrons). These parameters are measured and tuned to meet the requirements. The measurement procedures are discussed and the results are presented in this section.

3.1 Non-linearity

A detector is said to be linear if the ratio of output CCD counts to input photon counts is constant for any given input photon count value. In practical applications, a detector needs to be linear throughout its dynamic range but there could be a small fraction of non-linearity present (around 1 per cent). It is important to analyse the degree of non-linearity that is present in the detector pixels. The non-linearity was measured using the photon transfer technique. A series of images with stepped exposure times and fixed illumination were acquired. The output of the CCD camera was in the normal operating range of 15 000–150 000 electrons per pixel. Fig. 6 is the photon transfer curve (PTC) of the CCD camera read at 280 kHz pixel readout rate and gain value of 3 electrons per ADU. The non-linearity is measured using the equation (1).

Non-linearity

$$= \frac{|Max\ positive\ dev| + |Max\ negative\ dev|}{|Max\ intensity|} \quad (1)$$

The magnitudes of maximum positive and negative deviations from the straight line fit are measured and the non-linearity is calculated. The maximum intensity is the maximum pixel value

Table 2. Measured non-linearity values of the four readout channels of the CCD.

Channel	E	F	G	H
Non-linearity (per cent)	0.64	0.62	0.52	0.59

recorded on the CCD for this test. The estimated values of the non-linearity (in per cent) of the CCD are given in Table 2. The measured non-linearity in all the readout channels was under 1 per cent. These results concluded that CCD has a linear response in the normal operating range of 15–150k electrons per pixel.

3.2 Charge transfer efficiency

The CTE is the efficiency at which charge is transferred in the CCD registers during the readout. It depends on various parameters like readout frequency and operating temperature (Moshen & Tompsett 1974; Hopkins, Hopkinson & Johlander 1995; Hardy, Murowinski & Deen 1998). The charge packets are required to undergo several thousands of transfers before they are read and hence must be transferred very efficiently. The CTE value, thus, should be very high, i.e. close to 1 (100 per cent). A lesser CTE means there is a loss in charge during the transfer and hence the pixels that are away from the readout channel will lose a considerable amount of charge by the time they are read out. The inefficiency in charge transfer is expressed as charge transfer inefficiency (CTI) which is given by $CTI = 1 - CTE$. The CTE is defined as

$$E^n = 1 - C, \quad (2)$$

where E is CTE, n is the number of transfers and C is the fraction of the mean charge lost.

To measure the CTE, the CCD was exposed to a ^{55}Fe radioactive source. A ^{55}Fe atom decays into an Mn atom and in the process produces $K\alpha$ and $K\beta$ photons. The absorption of these X-ray photons by the CCD detector produces 1620 and 1778 electrons, respectively. Each photon hit that corresponds to these electrons will be converted into ADUs in the output image, depending on the gain of the readout channel. The pixels which are hit by these photons are referred to as hit pixels while the others are called background pixels. After a long duration exposure (100 s), the CCD is read from a single channel readout. About 20 000 hit pixels will be formed during this time. These hit pixels contain single hits, partial hits, and multiple hits. Two regions of size 4000×300 pixels, one nearest and the other farthest from the readout direction are considered, and the mean intensity values of hit pixels from these two regions is calculated. The ratio of these mean values from the far region to the near region gives the fraction of charge lost ‘ C ’ and the mean distance between these two regions gives the number of extra transfers ‘ n ’. Then, the CTE ‘ E ’ was measured using the aforementioned formula. Both serial and parallel CTE were measured by considering regions near and far from the readout direction along the rows and columns, respectively, as shown in Fig. 7. The measured CTE values are tabulated in Table 3. The measured serial and parallel CTE values are high and comparable to those specified by the CCD provider.

3.3 Image cross-talk

Modern CCDs operate mostly in multichannel readout modes and at a high pixel readout rate. Such parallel readout exhibits a problem called image cross-talk. This problem develops when two or more

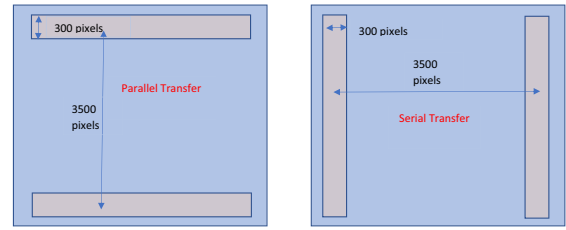


Figure 7 Image sections considered for calculating parallel and serial CTEs. One section is taken nearest to the readout channel while the other is taken farthest.

Table 3. Measured serial and parallel CTE values.

Serial CTE (per cent)	99.99991 ± 0.00003
Parallel CTE (per cent)	99.99992 ± 0.00002

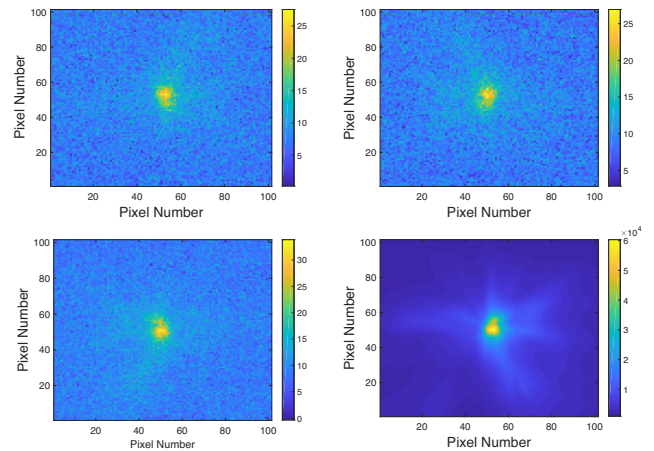


Figure 8 Images showing cross-talk among the four quadrants. The bright source in channel F (bottom-right panel) induces cross-talk in the remaining channels appearing as a ghost image.

channels are reading the CCD simultaneously, producing ghost images between channels. When a bright source is present in one of the quadrants, in the case of a CCD with four read-out channels, a ghost image appears in the remaining three quadrants of the imaging region in the CCD after readout. This is due to the cross-talk induced during simultaneous clocking operations using the same clock chain. Understanding and measuring the cross-talk is important for evaluating both the sensor performance and the readout electronics efficiency. Also, it is important to keep this cross-talk as low as possible. Since *SUIT* has a four-channel readout, cross-talk from one channel will be induced in the remaining three channels. The cross-talk from a channel was measured by focusing a bright source on a small region in one channel (quadrant) and measuring the effect of this on the remaining channels (Freyhammer et al. 2001). The source is bright enough to near saturate the pixels (around 60 000 ADUs). The mirror regions in the remaining three quadrants were taken and the intensity over the background was measured. Fig. 8 shows the cross-talk-induced regions along with the source region in the four quadrants of the CCD. The ghost images produced in the remaining three quadrants due to the near-saturated image in one of the quadrants are seen here. The cross-talk is estimated from these images as the ratio of the increase in intensity in other channels to the intensity of the bright region in the source channel. The cross-

Table 4. Measured cross-talk values (number of cross-talk induced electrons per 10 000 electrons in source channel) in each channel due to near saturated region on other channels.

	E	F	G	H
E	NA	1.8 ± 0.3	0.6 ± 0.2	0.8 ± 0.2
F	1.5 ± 0.3	NA	0.6 ± 0.2	0.5 ± 0.1
G	0.5 ± 0.2	0.6 ± 0.2	NA	1.0 ± 0.02
H	1.4 ± 0.3	1.0 ± 0.3	1.7 ± 0.3	NA

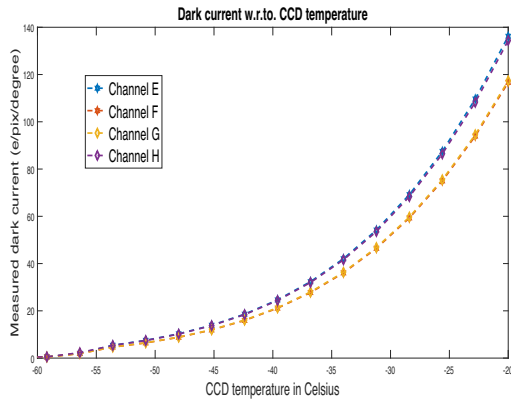


Figure 9 A plot of dark current in the four channels with CCD temperature. The dark current is under five electrons per pixel per second when the operating temperature is under -55° Celsius.

talk from the readout channel of a given quadrant induced in the remaining three channels is estimated for each channel and the values are tabulated in Table 4. The measured cross-talk values are within the acceptable range.

3.4 Dark current

Dark current, as the name suggests, is due to the electrons produced in the pixel wells without any external light illumination. This comprises electrons that are thermally excited from the valence to the conduction band and are stored within the pixel well, over time. A high value of dark current reduces the dynamic range of the CCD. The dark current depends on the operating temperature and increases with an increase in the exposure time. The temperature dependence of dark current was discussed in McGrath et al. (1987), Mccolgin et al. (1992). The dark current signal increases with temperature exponentially (Widenhorn, Dunlap & Bodegom 2010). Hence, it is required to cool the CCD to minimize the dark current. Dark current is measured as a mean value of dark images (images taken with a closed shutter). To measure dark current at various temperatures, dark images are taken with an exposure time of 100 s at different CCD temperatures from -20 to -60° Celsius. The dark current is calculated using these images and plotted in Fig. 9. It can be seen that once the CCD is cooled beyond -55° Celsius, the dark current has become almost negligible (inside the noise floor). Hence, it was decided to cool the CCD to under -55° Celsius to minimize dark current.

4 ANALOGUE ELECTRONICS TESTING

The *SUIT* analogue electronics consist of a clamp-and-sample-based CDS circuit for signal sampling. An offset voltage is added to the sampled value using a DAC. The analogue signal is then amplified using a programmable gain amplifier and is digitized using an ADC.

In this section, the gain values produced by the programmable gain amplifier are measured and tuned according to the specifications. The DAC input voltage is also tuned to produce the required bias value at the output. All these components present in the analogue chain produce noise which is also measured and presented.

4.1 Gain

The gain corresponds to the ratio of the number of electrons recorded by the CCD to the number of digital units (counts) produced at the output. The overall gain accounts for several stages in the signal path like quantum efficiency of the CCD, the sensitivity of the pixels, stages of electronic amplification, analogue to digital conversion, and pixel computation. The gain value is decided based on the full well capacity of the CCD and the number of ADC bits. The *SUIT* CCD has a full well capacity of 190 000 electrons which is almost three times the number of ADC bits for a 16-bit ADC. So, an electronic gain value close to 3 (gain setting 1) is used to get the highest possible dynamic range and will be used while observing high-energy events like flares. Also, two other gain settings (2 and 3) correspond to gain values of 1.6 and 1, respectively are also included. The gain value 1 gives the best possible detection resolution of one electron and will be used while observing the quiet Sun. It is to be noted that the gain that is mentioned here is defined as electrons per ADU. So, it can be understood as an inverse gain. Hence, a gain of '3' means, three electrons are converted into 1 ADU (low system gain) at the output and hence we use gain value 3 to utilize the full well capacity, which is approximately three times the ADC range. Similarly, gain '1' means, one electron is converted into 1 ADU (high system gain) and hence this gain setting will give the best resolution of one electron detection. These gain values need to be measured accurately to be able to specify fundamental system parameters such as noise, dark current, full well capacity, etc., using fundamental charge units (electrons).

There are several methods used to measure the gain of a CCD system. One of the well-known ones is based on the PTC, which requires exposing the CCD to a light source and measuring the signal and noise response of a group of pixels when the sensor is operating under limited shot noise conditions (Janesick 2007). The other well-known method (employed in this analysis) uses a ^{55}Fe X-ray source (Rodrigues et al. 2021). The absorption of the X-ray photons by the CCD produces 1620 and 1778 electrons in Silicon, respectively. Each photon hit that corresponds to these electrons will be converted into ADUs in the output image, depending on the gain of the readout channel. The ratio of the number of electrons produced by an X-ray photon hit to the mean ADU value produced gives the value of electronic gain. In this measurement, the CCD was exposed to a ^{55}Fe X-ray source and long-exposure images were taken. A histogram of the pixel values of the images was plotted and the peaks corresponding to the X-ray hits were then identified and fitted with a Gaussian function. Fig. 10 shows the two peaks in the histogram plot corresponding to $K\alpha$ and $K\beta$ photons along with the bias peak. This histogram was obtained by using a 4-pixel binning and hence the original ADU value will be four times what is shown in the plot. The position of the Gaussian peak represents the value of the photon hit pixels in ADUs. As mentioned earlier, the ratio of the number of electrons (1620/1778) to these ADU values determines the electronic gain of the system. The gain values for each gain setting are measured and presented in Table 5. The three required gain values are obtained and the differences in gain values between each channel for a given gain setting are within the acceptable tolerance of 2 per cent.

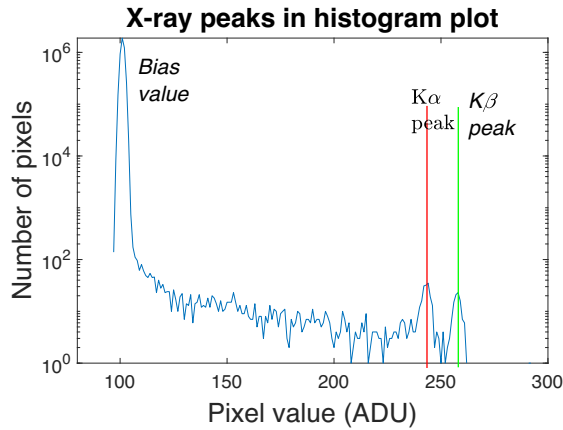


Figure 10 Histogram plot showing the X-ray peaks from the ^{55}Fe used for gain measurement. The x -axis corresponds to value in ADUs binned by 4 pixels.

Table 5. Measured gain values in electrons per ADU for three different gain settings.

Gain	E	F	G	H
1	3.04 ± 0.02	3.09 ± 0.01	3.01 ± 0.02	2.95 ± 0.02
2	1.61 ± 0.01	1.64 ± 0.01	1.60 ± 0.02	1.63 ± 0.02
3	0.99 ± 0.01	1.0 ± 0.01	0.99 ± 0.01	0.96 ± 0.02

Table 6. Offset DAC values that are optimized to achieve desired bias count values and corresponding average bias values, respectively, given for each channel, for different gain settings.

Gain value	3	1.6	1
Channel	DAC, bias	DAC, bias	DAC, bias
E	132,144	130,135	130,164
F	134,113	133,164	133,198
G	134,112	133,170	133,215
H	130,114	129,171	129,205

4.2 Bias and offset

The input offset voltage determines the output mean bias value of the CCD. The offset voltage is generated using an 8-bit DAC and the range of this voltage is 2.5 to 3.75 V. For a given gain setting, the offset voltage needs to be tuned to produce optimum bias value at the output. This bias value should be such that the CCD counts will always remain positive despite the RMS noise fluctuations. Hence, the bias value should be at least 10 times the expected readout noise value (which is around 10 electrons). The output bias value for different offset voltages (controlled using DAC) is found and their relationship is established. Then, the bias value is optimized to be in the range of 100–200 ADUs and the corresponding DAC value is calculated. Also, the mean bias values across the four channels are adjusted to be uniform. The optimized DAC values and the corresponding CCD bias counts are given in Table 6.

4.3 Readout noise

The total system noise comprises noise from several sources including signal shot noise, readout noise, and fixed pattern noise (Holst 1998). The read noise corresponds to the noise produced during the readout. It is made up of reset noise, amplifier noise, and digitization

Table 7. Measured readout noise values for three different gain settings.

Gain value	3	1.6	1
E	8.17 ± 0.04	7.02 ± 0.04	6.57 ± 0.01
F	8.24 ± 0.04	7.11 ± 0.03	6.66 ± 0.01
G	8.59 ± 0.06	7.43 ± 0.05	7.04 ± 0.01
H	9.40 ± 0.04	8.86 ± 0.09	8.12 ± 0.02

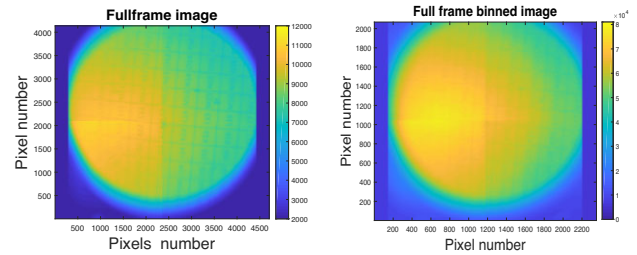


Figure 11 A normal full-frame image (left-hand panel) and binned full-frame image (right-hand panel) were taken using a four-channel readout.

noise. It is independent of the exposure time and the source intensity. This read noise limits the sensitivity of the instrument and hence must be kept as low as possible. One of the most popular methods to derive the readout noise value is to make statistics of the standard deviation of bias image or overscan area in a normal image. In this analysis, images are taken with 254 overscan pixels on either side of each row. This overscan region is used to calculate the readout noise. The measured read noise values at different readout channels and gain settings are given in Table 7. Gain settings ‘1’, ‘2’, and ‘3’ correspond to gain values 3, 1.6, and 1, respectively. The readout noise is under 10 electrons meeting the required specifications.

5 TIMING ELECTRONICS TESTING

The timing electronics package is primarily used to provide required clocks to read the CCD in different readout modes. Along with a normal full-frame image and a full-frame image with 2×2 -pixel binning, different sizes of RoI images at different positions on the CCD can be read through all the readout modes. The required clocks have to be generated depending on the size and position of the RoI and the readout mode. All these aspects are discussed and their test details are presented in this section. The timing electronics package also contains an LED current driving circuit to drive 16 LEDs placed on the LED panel which are used for flat fielding. This LED control circuit is also tested and the results are presented in this section.

5.1 Full-frame and binned image

A normal full-frame image and a full-frame image with 2×2 -pixel binning were captured and studied. This is to ensure that all the rows and columns in the image are read out properly and also the pixel values are stored in the correct address locations of the SDRAM and are retrieved accurately. Any error in clocking or while retrieving pixel data from SDRAM will produce an erroneous pattern in the image. The images captured were studied to make sure they are captured and read properly. Fig. 11 shows both the normal (left-hand panel) and binned (right-hand panel) full-frame images taken using a four-channel readout. The sides of the image are visibly chopped due to the smaller aperture size of lens 2 as shown in Fig. 1.

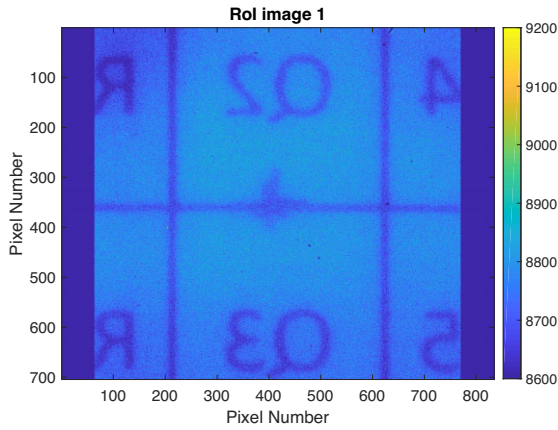


Figure 12 A sample ROI image obtained from a four-channel readout.

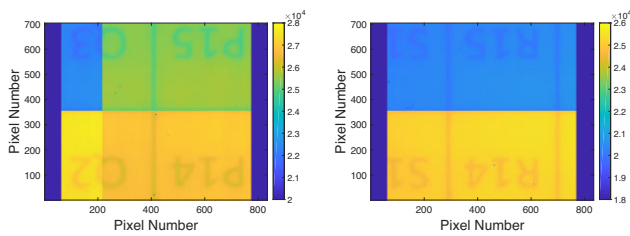


Figure 13 Sample ROI images that were taken using four-channel (left-hand panel) and two-channel (right-hand panel) readout modes.

5.2 ROI image

This test aims to read ROI images of various sizes and at different positions on the CCD. The ROI images were selected such that they cover every part of the CCD and take care of all the boundary conditions where different parts of the ROI image are read from two or more readout channels. A total of 211 ROI cases were chosen, that fulfil all the required test conditions. These include different ROI positions and sizes. Both square and rectangular ROIs with sizes ranging from 128 to 1024 pixels are considered. All the ROI images corresponding to these test cases were obtained and verified by comparing them with the expected ROI image cropped from the full-frame image, using the ROI coordinates. This test ensures that all possible ROI positions and sizes are read successfully. Fig. 12 shows a sample ROI image obtained through the four-channel readout.

5.3 Readout modes

The *SUIT* CCD can be read simultaneously using four readout channels. Also, any one or combination of these readout channels can be used for the readout. Table 8 shows the 11 readout modes used in *SUIT*. The normal and binned full-frame images and 215 cases of ROI images mentioned in the previous two subsections were obtained using all these 11 readout modes and the images are verified. Fig. 13 shows sample ROI images read out using the four-channel and two-channel (EH) readout modes.

5.4 LED testing

All 16 LEDs were tested individually and also in groups. The LED panel was placed at the image plane and their focused images were taken using the detector as shown in Fig. 5. This set-up is different from the original *SUIT* optical set-up. On the *SUIT* optical test bench,

Table 8. List of different readout modes and the corresponding readout channels in *SUIT*.

Readout mode	Readout channels
1	E
2	F
3	G
4	H
5	E,F
6	E,G
7	E,H
8	F,G
9	F,H
10	G,H
11	E, F, G, and H

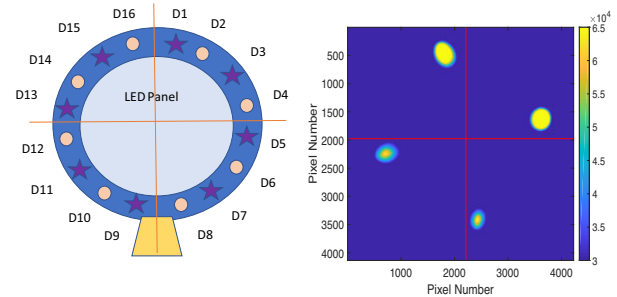


Figure 14 The image on the left hand shows how the LEDs are placed on the LED board. It is used to verify if the LEDs are glowing as per the sequence. The star symbol represents the 255 nm LEDs and the circle represents the 355 nm LEDs. As seen, these two sets of LEDs are placed alternatively. The image on the right hand corresponds to case 9 where LEDs 4, 8, 12, and 16 are turned on.

the LEDs will be placed in an out-of-focus position. The efficiency of flat fielding is yet to be tested on the ground and will be discussed elsewhere. The aim of this set-up was not to test how the flat fields are generated but to test if the LEDs are switching on and off as commanded. Hence, only for this test, the LEDs were focused on the detector plane. All the LEDs were driven in a specific sequence and the corresponding images were taken. These images were used to verify if the LEDs glowed as per the sequence.

Fig. 14 (left-hand panel) shows the position of how the LEDs are arranged on the panel. The obtained image is compared with this reference image for verification. Fig. 14 (right-hand panel) shows a sample output image corresponding to LEDs 4, 8, 12, and 16 on. It was observed that all four LEDs were glowing as expected.

6 SUMMARY AND CONCLUSIONS

The CCD was characterized and the readout electronics package was tested. The CCD characteristics like linearity, dark current, cross-talk between different readout channels, and CTE were measured and the values were found to meet the required specifications. The overall non-linearity in all the channels was less than 1 percent. In the operation range of -55 to -60° Celsius, the dark current produced was under 2 electrons per pixel per second. Also, a cross-talk of around 1 electron per 10 000 electrons was present in all the channels. The CTE was very high with both serial and parallel transfer efficiencies of more than 99.9999 per cent. The readout electronics specifications like noise, gain, and bias were also met. A read noise of under 10 electrons in all channels was achieved. The

required gain values are obtained within a tolerance of 1 per cent. The bias value was tuned in the range of 100–200 ADU in all gain settings. The timing electronics package was tested by taking full-frame, bin, and RoI images in all 11 readout modes. The LED driver in this board was also tested successfully. All the functionalities in the processing electronics package, namely HELIOS flare trigger, flare localization, RoI tracking, and automatic exposure control were successfully tested.

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DATA AVAILABILITY

The data underlying this article are provided in the article where ever possible. Other data if required will be shared on reasonable request to the corresponding author.

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