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FPGA Based ASM implementation for CCD Camera Controller

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Abstract

A general purpose CCD controller that can address any CCD, has been developed at the Indian Institute of Astrophysics. It is based on a Digital Signal Processor (DSP) chip, Motorola DSP 56002 for implementing essential operations such as read-out of the CCD, interfacing with the host and correlated double sampling for reset noise elimination. In order to reduce the chip count and size of the controller with a view to adopt it for building a space borne application of the camera, a need has been felt to implement the design with the use of a Field Programmable Gate Array (FPGA) approach. Such an approach would not only be efficient but would also be able to enhance the image processing strategies. After examining the functionality of the DSP board, Bias and Clock board, Host Interface and Data Acquisition functions, an Algorithmic State Machine (ASM) is derived from the DSP code. In this paper we report the ASM design that has been used to design the system using the Hardware Description Language (HDL). Verilog HDL is used to create the code, which can be tested and debugged using Xlinx ISE software package. This paper also reports the timing generator that has been implemented on Xlinx chip. It is proposed to implement the serial and parallel communication with fibre optics link in this approach.

1. Introduction to Front-end Camera Electronics:

Indian Institute of Astrophysics had earlier developed a DSP based CCD camera controller. Since component-reduction, power reduction, enhanced reliability and easy reprogram ability are desirable features, in a camera design for space applications, a new approach based on FPGA design was taken up.

1.1 DSP Based Camera System

It is appropriate to describe the Hardware architecture of the DSP based camera system, before the FPGA approach can be listed. The controller architecture is based on a host computer centered on a PC and a front end electronics implemented with a DSP. The camera system comprises of the following major units.

- Dewar housing the CCD, in a cryogenic environment
- DSP CPU board
- Bias and Clocks Board
- Analog Signal Processing Board
- Pre-amplifier Board
- Host interface Board

The communications between the host computer and the camera controller (for bootstrapping commands) is implemented through a serial communications link (Tx, Rx, Clock) while the CCD data acquired by the DSP controller, is transferred to the host computer through an 8-bit parallel port. The host environment is shown in Figure 1.

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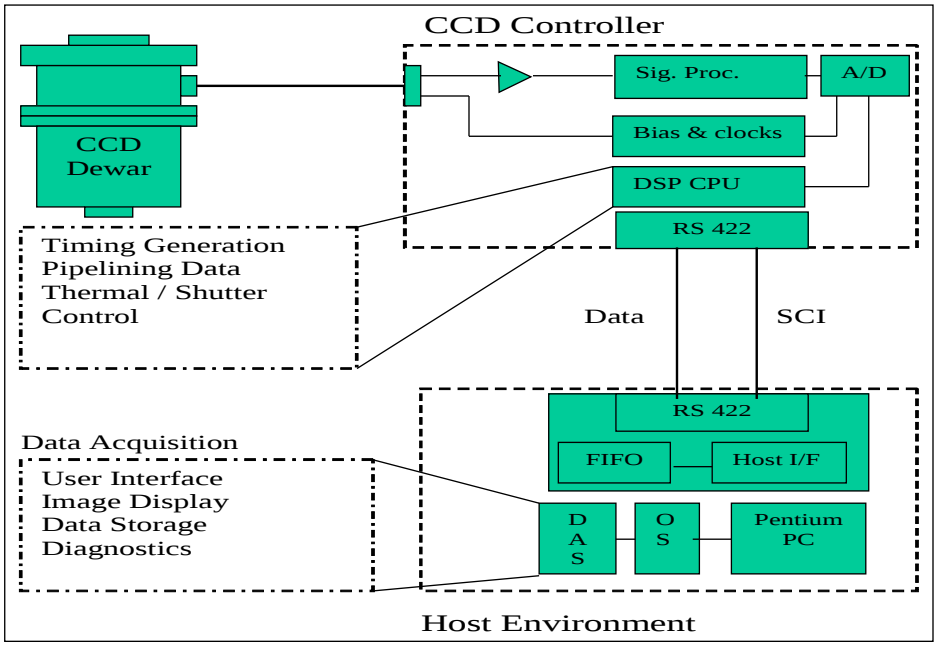

2. Host interface interaction in FPGA:

2.1 FPGA as Front-End Controller

In the new architecture developed a FPGA replaces the DSP and forms the front-end camera controller. The VHDL generates a formatted file called **Bit file** when assembled. This file can be read to pick up the program address and the code to be loaded in to FPGA. Once the FPGA is loaded with the bootstrapping code, the FPGA executes the program from the starting location in the program memory. The program then waits in a loop to receive serial commands from the host computer. The serial commands are of 24 bits width and when a command is received, the FPGA acknowledges the host by sending a pattern “AA” back to the host after execution of the command.

2.2 Role of FPGA

VHDL code is written using the state machine and state transitions as required in the CCD controller. The functions of CCD camera electronics are categorized in terms of states and libraries available in the IEEE are used in this implementation. In VHDL an entity declaration gives a name of the entity and what is defined in its interfaces facilitates communication to the outside world in terms of a list of ports. This program uses the process statements. Process statement starts at time 0 and the controller program executes the statements in the process block continuously in a loop. Process statements are concurrent. So, all the process statements will be executing simultaneously. All the state functions as described in a process, are running in parallel. Hence, it increases the speed of execution.

2.3 Description of one of the ASM states (State-7)

In order to describe a typical ASM signal-flow, one of the states (State-7) is described. The State-7 is used to read a given rows, with the required binning factors for the rows and the columns. When control bit (a1 (22)) is set, the control will be given to state-7 after clearing the control bit. The row binning is performed, by reading the required number of row bins from the passed on parameters. The idea is to commence the serial shifts after the set number of binned-rows is shifted into the read-out register. In a similar way, the required serial number of bins is used, during the serial shifting of the read-out register, before the ADC conversion is initiated. The binned serial shifted charges are held in the output capacitor, till the digitization is performed. The pre-scan and post-scan parameters are utilized in acquiring the region of interest.

2.4 List of ASM States:

State assignment

STATE	CODE	NAME
T0	0000	IDLE
T1	0001	BOOTSTRAP
T2	0010	LOADDAC
T3	0011	OUTDATA
T4	0100	CLRROWS
T5	0101	PREFLUSH
T6	0110	GETPAR
T7	0111	READROW
T8	1000	PRESHIFT
T9	1001	STRBDATA
T10	1010	POSTSHIFT
T11	1011	RESET

Table T1

State Transition Table

PRESENT STATE	Asserted Input /Signal	Next State
T0	START	T1
T1	A1[16]	T2
T2	A1[17]	T3
T3	A1[18]	T4
T4	A1[21]	T5
T5	A1[19]	T6
T6	A1[22]	T7
T7	((NOOFBROWS!=0)&&~PBIN &&~PRESCAN	T8
T8	~iSSO	T9
T9	~BNSERIAL	T10
T10	~iPOSTSHIFT	T7
T7	((NOOFBROWS=0)&&A1[20])	T11
T11		T0

Table T2

3. Camera Waveform Generation with FPGA:

The waveform contains the levels of 16 state bits at any given time. The patterns are time sliced and time field is then combined with state field to produce a combined word (24bits). Sequences of such words are used to represent the parallel transfer, serial transfer or pre-flush waveforms. These words are inserted in the VHDL program in the waveform generation sub-routines. The control bits are set on the D15-D0 data bits of the FPGA.

The Double correlated sampling (DCS) technique eliminates the reset noise by taking two samples of the CCD signal per pixel, one before and one after the charge packet is shifted to the node capacitor. The reference signal is positively integrated (SBIT11 low) for a defined period of time (SBIT12 low) and after the charge shift, the signal is negatively integrated (SBIT11 high) for the same time. The resulting output at the integrator is proportional to the detected signal and is free from the reset noise. The integration also smoothens high frequency noise. The integrator has been configured for a gain of 5microseconds.The DCS integration time and thereby the integrator gain can be varied using the state bit (SBIT12) of the signal processing control bits.

3.1 Waveform generation is implemented in Xilinx version 10.1 and is shown below.

Figure3.1 Parallel Waveform

4. Communication FPGA

In the DSP architecture, the communication link was implemented with a serial link for sending commands to CCD camera electronics and the transfer of image data from the camera electronics to the host using parallel data-transfer with a strobe. In the new architecture the serial and parallel copper wire link is replaced, with a high speed fiber optic link. Apart from speeding up the communication, the noise interference to the data transmission is greatly reduced in this approach.

5. Conclusion

This paper reports the use of FPGA as an alternative to the DSP controller, currently in use in the CCD Camera System at the Indian Institute of Astrophysics. The FPGA implementation of the DSP controller offers significant improvement in terms of small size, enhanced reliability and low power consumption. With this improved features, this camera controller becomes suitable for space applications.

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