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A New Digital Display System for the 1-m Telescope at Vainu Bappu Observatory

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ABSTRACT. The Carl Zeiss 1-m telescope at Vainu Bappu Observatory uses synchro transmitters as angular transducers in a three-stage geared train for the two-axis coordinate display system. Synchro-receivers are used in the console with analog dials displaying the position coordinates. In this approach the transmitters exhibit good performance and the receivers often suffer from dial sticking, thereby resulting in ambiguous and inaccurate readings. The original Carl Zeiss display system has a resolution of about 15 and 30 arcsec in RA and DEC axes, respectively. A new digital display system has been developed which replaces the synchro receivers with suitable electronics while retaining the synchro transmitters. This approach has resulted in better resolution (1.25 and 2.5 arcsec for RA and DEC, respectively) and accuracy over the analog dial display. This paper presents the hardware and software details of our implementation.

1. INTRODUCTION

The original coordinate display system of the 1-m Carl Zeiss telescope at VBO used synchro transmitters for the RA and DEC axes. Three synchros for each axis are used in a geared configuration for each axis to enhance the resolution of the display system. Synchro receivers are used with dials to follow the transmitters. There is an increasing trend in inaccuracies of the readings while the dials suffer problems like sticking, lagging behind due to their inertia, etc. One possible solution would be to replace the synchro transmitters with optical encoders of the required resolution. This approach would require mechanical modifications to replace the synchro transmitters with optical encoders and space constraints do not permit this solution. The modern electronic Scott-T converts synchro signals to resolver format and monolithic resolver-to-digital converters (RDC) are available. This allows a low-cost, high-resolution, and high-accuracy approach to the digital display system while retaining the synchro transmitters. In this paper, the hardware and software details of our new approach are presented. The resolution and accuracy realized in this approach are analyzed and the performance obtained is indicated.

2. PRINCIPLE OF OPERATION AND SYSTEM OVERVIEW

The principle of operation of a synchro used as an angular transducer is based on the inductive coupling between a rotor and three sets of stator windings. The rotor is excited with an ac reference voltage and a set of unique induced voltages is generated in the stator windings for a given position of the rotor. The three stator windings are connected in a "Y" configuration and are spaced 120° apart. When the rotor is excited with a reference voltage of the form $A \sin(\omega t)$, the voltages induced across the stator terminals are

$$S1-S3 = A \sin(\omega t) \sin(\theta),$$

$$S3-S2 = A \sin(\omega t) \sin(\theta+120),$$

$$S2-S1 = A \sin(\omega t) \sin(\theta+240),$$

where θ is the synchro shaft angle. These synchro voltages are converted into resolver format of the form below using an electronic Scott-T circuit:

$$S1-S3 = A \sin(\omega t) \sin(\theta),$$

$$S2-S4 = A \sin(\omega t) \cos(\theta).$$

The resolver signal is digitized by a RDC. In a three-stage geared configuration, three electronic Scott-T circuits and three RDCs are used for each axis. The RDC values are read through synchronizing logic to obtain an unambiguous high-resolution shaft angle reading. A PC input port reads the HA and DEC encoders and local sidereal time through a suitable multiplexer. The PC computes the RA and DEC coordinates and parameters like zenith distance and air mass and displays the values on the monitor.

2.1 Resolver-to-Digital Conversion Principle

A tracking converter is utilized to implement the RDC (Analog Devices AD2S80) and is based on an electronic type-2 servo loop for its operation. The resolver format voltages $V1$ and $V2$ are applied to sine and cosine multipliers to produce

$$V \sin \omega t \cos \theta \sin \varphi$$

and

$$V \sin \omega t \sin \theta \cos \varphi,$$

where φ is the digital angle. The signals are subtracted by the error amplifier to give the error signal:

$$V \sin \omega t(\sin \theta \cos \varphi - \cos \theta \sin \varphi) = V \sin \omega t \sin(\theta - \varphi).$$

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The error signal is fed into an integrator and the output drives a voltage-controlled oscillator (VCO). The VCO outputs pulses to an up–down counter until

$$\sin(\theta-\varphi) = 0.$$

At this point, $\theta-\varphi=0$ or $\theta=\varphi$. Therefore the internal loop will null when the digital angle φ equals the shaft angle θ. The converter does not require any external start convert command and tracks the input. The parameters (bandwidth, maximum track rate, and velocity scaling) of the converter can be set with the selection of external resistor and capacitors (data Sheets, 1990 and application software, 1990) to suit a particular system.

2.2 Synchronizing Logic

The synchronizing logic resolves the conflict in the overlapping bits of the coarse/fine digital readings and provides an unambiguous digital output. To illustrate the logic, let us consider a simple example of a coarse/fine system with a binary gear ratio of 1:16 (coarse:fine). If a zero backlash error can be assumed, then the fine output data can be scaled to give them correct bit weights in terms of coarse-shaft angle. Depending on the resolution of the R/D converters there will be an overlapping region in the two readings where the digits will correspond to each other. Assuming a fine RDC resolution of 12 bits and coarse RDC of 10 bits, 10° of coarse rotation will result in 160° of fine shaft rotation. The best possible representation of these angles in natural binary will be

Coarse-shaft angle: 0 0 0 0 0 1 1 1 0 0

Fine-shaft angle: 0 1 1 1 0 0 0 1 1 1 0 0

By shifting the fine readings by four places to the right (gear ratio is 2^n, $n=4$), the overlapping bits correspond to each other. Then the combined word (16 bits) represents the coarse-shaft angle of 10°:

			n		C	D										
Coarse-shaft data:	0	0	0	0	0	1	1	1	0	0						
Fine-shaft data(shifted):					0	1	1	1	0	0	0	1	1	1	0	0
					A	B										
Combined (16 bits) word:	0	0	0	0	0	1	1	1	0	0	0	1	1	1	0	0

where A=Most significant bit of fine data,
B=Next most significant bit of fine data,
C=(n+1)th significant bit of coarse data,
D=(n+2)th significant bit of coarse data.

In a practical design where there is backlash and cyclic errors due to gearing imperfections, the overlapping digits will not change alike at the transition points. There will be ambiguity in combining the two digital readings.

A synchronizing logic (Boyes 1980) eliminates the ambiguity of the overlap bits and is based on the following assumptions:

(1) The fine-shaft data gives the best representation of the coarse-shaft position.
(2) The backlash, cyclic errors, etc., which cause the ambiguity is not greater than the bit weight of digit D on the coarse-shaft data.

This logic operation uses digits C and D on the coarse-shaft data and the two MS bits A and B on the fine-shaft data. The synchronizing logic operation and the truth table are shown in Table 1. A 16-bit word is obtained by combining the four MS bits of the coarse-shaft data after they are modified by the synchronizing logic and the 12 bits of the fine-shaft data.

In the case of nonbinary gear ratios the coarse data is multiplied by the gear ratio to have similar bit weights to that of binary gear ratio case. After modifying the overlapped bits by the synchronizing logic, the data are rescaled to have the correct bit weights.

2.3 Three-Speed Coarse/Fine Systems

A three-speed coarse/fine combination system is used on the HA and DEC axis to measure accurately the position of the telescope. At the receiver side the outputs from the coarse/fine shafts need to be digitized and combined to provide a single digital word representing the coarse-shaft angle. With the existing gear ratios 1:24 and 1:30 for HA and 1:12 and 1:30 for DEC axes, a suitable synchronizing logic is developed to achieve 20 bits for HA and 19-bit resolution for DEC axis. A block diagram of the three-speed coarse/fine system is shown in Fig. 1.

The flow chart of the synchronizing logic for the three-speed system is shown in Fig. 2. The very fine shaft is digi-

TABLE 1
(a) Synchronizing Logic Operation and (b) Truth Table with Carry or Borrow from Logic Operation

a.	*A*	*B*	Operation on Digit *D*
	0	0	+1
	1	1	−1
	0	1	0
	1	0	0

b.	*AB* / *CD*	00	01	10	11
	00	0	0	0	−1
	01	0	0	0	0
	10	0	0	0	0
	11	+1	0	0	0

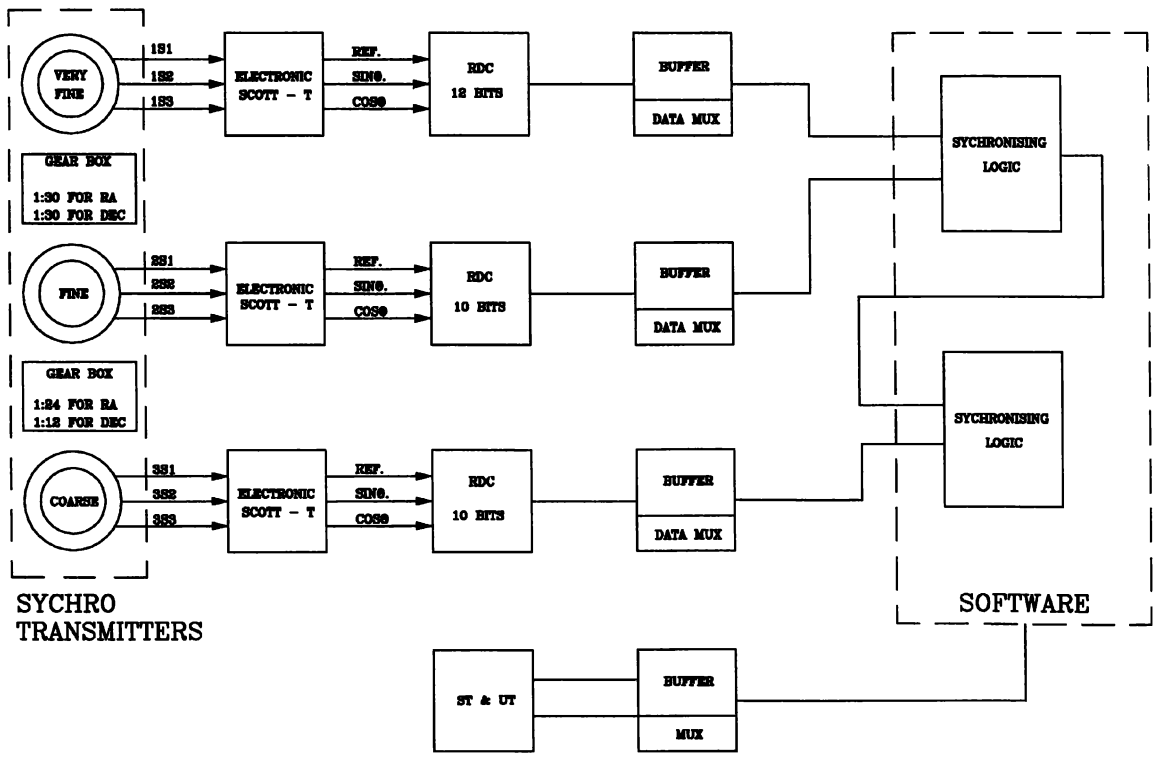

FIG. 1—Block diagram of the display system.

tized to 12 bits and the fine and coarse shafts are digitized to 10 bits each. The fine data are multiplied by 30 (the gear ratio between very fine and fine is 30:1) to shift the fine data to the right. Since the synchronizing logic requires only seven MS bits, the remaining bits are ignored. The five MS bits of the fine data (after they are modified by the synchronizing logic operation) are combined with the very-fine-shaft data which is then rescaled to have the correct bit weights before providing the 16-bit data that represent the fine-shaft angle. Similarly the coarse data are combined with the resultant 16-bit fine data to produce a 20-bit datum that represents the coarse-shaft angle for RA axis. A 19-bit resolution is obtained for the DEC axis.

3. HARDWARE DESCRIPTION

3.1 Electronic Scott-T Circuit

Since the monolithic resolver-to-digital converter (RDC) works with resolver format signals, it is necessary to convert the synchro input signals to resolver form. Conventionally these transformations are carried out by using a pair of transformers known as Scott-T transformers [Fig. 3(a)]. The ratio of turns between primary and secondary is 1:1 for the main transformer and $1:2/\sqrt{3}$ for the teaser transformer in order to perform the conversion. The tapping point of the main transformer is midpoint. A solid-state Scott-T circuit [Fig. 3(b)] employs operational amplifiers with suitable gains to perform this conversion. The attenuating resistor network brings down the high-voltage (90 V rms) synchro signals to a manageable low-level (2 V rms) voltage.

3.2 Modification to the Reference Voltage

When an analog dial display is used, a dither (modulated) voltage is introduced into the rotor signals of transmitters and receivers in order to enhance the reading accuracy of the dials. This modulated reference voltage is replaced with an unmodulated one while working with the RDCs.

3.3 Data Multiplexer

A data multiplexer is used to read the various digital information from the RDCs and the sidereal clock. A PC I/O interface card with a 16-bit digital in/out (I/O) lines (configured as two ports) is used for multiplexing the data into PC. The synchro-to-digital converter (SDC) card contains three individual Scott-T circuits along with the corresponding RDCs. An address decoder is also present on this card to select and read the data of each RDC. Two such SDC cards, one for the HA axis and one for the DEC axis, are used to read the position of each synchro shaft on the two axes. The LST and UT information available in BCD from an astronomical clock is also read through the multiplexer card.

3.4 Line Driver/Receivers

In order to allow about 30 m between the digital-display electronics unit located in telescope control room and the host computer sitting at the observing floor, a pair of line driver/receiver cards is used on the 16-bit digital I/O port of the host.

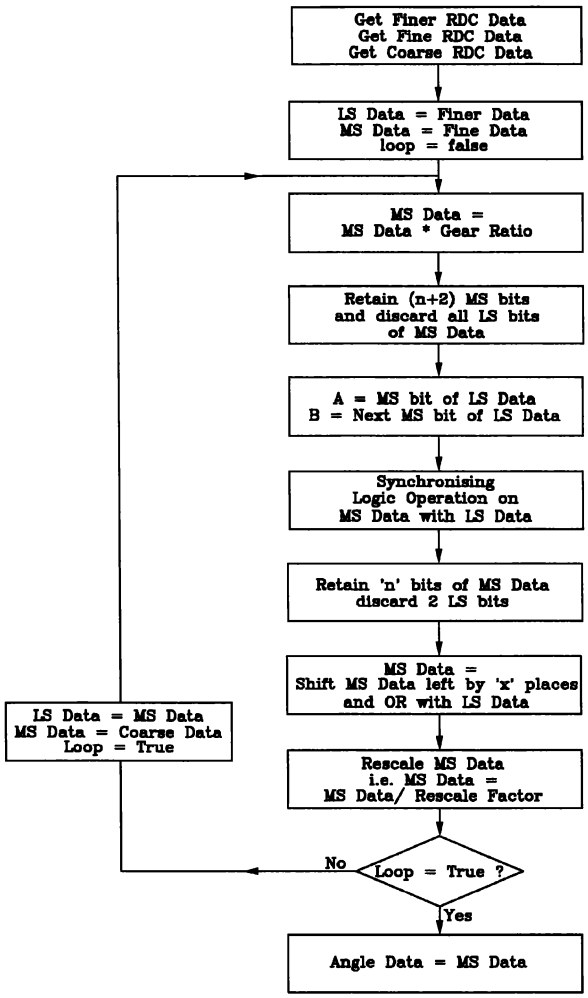

FIG. 2—Flow chart of three speed synchronizing logic.

4. SOFTWARE DESCRIPTION

The software for the display system is developed in Turbo-Pascal (the detailed software is available from the authors) and the program continuously loops through the following procedures:

(1) get RDC data,
(2) perform synchronizing logic,
(3) read clock, and
(4) compute coordinates and present to graphic display.

The software flow is depicted in Fig. 4.

4.1 GetRdcData (Address, Resolution:Integer; Var RdcData:Integer)

This procedure is used to read synchro data with the corresponding address and resolution parameters passed to the routine. The procedure gets the converted data of a synchro specified by the "Address" parameter passed by the program. "Resolution" indicates the number of bits to be read into the procedure. The procedure returns the RDC data to a variable "RdcData."

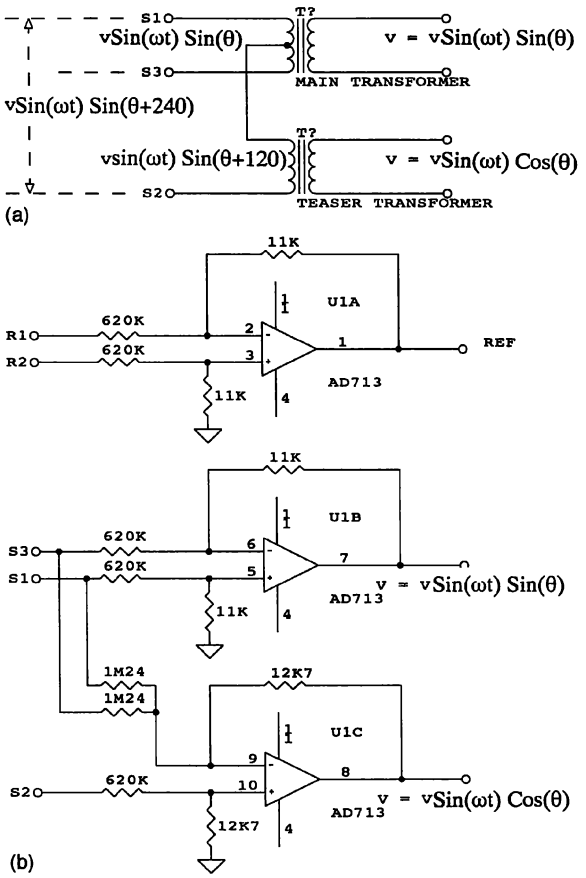

FIG. 3—(a) Scott-T transformer; (b) electronic Scott-T circuit.

4.2 SynchronizingLogic (Var IntAngle:Longint)

This procedure calls the "GetRdcData" procedure to get coarse/fine/very fine synchro-shaft data assigned to the variables; CoarseData/FineData/VeryFineData, respectively. The synchronizing logic is applied on the "FineData" and "VeryFineData" to get "FineAngle" which is rescaled to represent the fine-shaft angle with 16-bit resolution. The synchronizing logic is then applied on the "CoarseData" and "FineAngle" to get the "CoarseAngle" which is rescaled to represent the coarse-shaft angle with 20/19-bit resolution for the HA/DEC axis. The "CoarseAngle" is passed to the program as "IntAngle" of the long type integer. This "IntAngle" is multiplied by the corresponding LS bit weight to obtain HA/DEC in arcseconds.

4.3 ReadClock (Address:Integer; Var Time:integer)

This procedure is called with an "Address" parameter to get the fields of Local Sidereal Time (LST) and Universal Time (UT) information from the clock. The BCD data read through the I/O port are converted into decimals and returned to the variable "Time." The fields "LstHrs," "LstMin,"

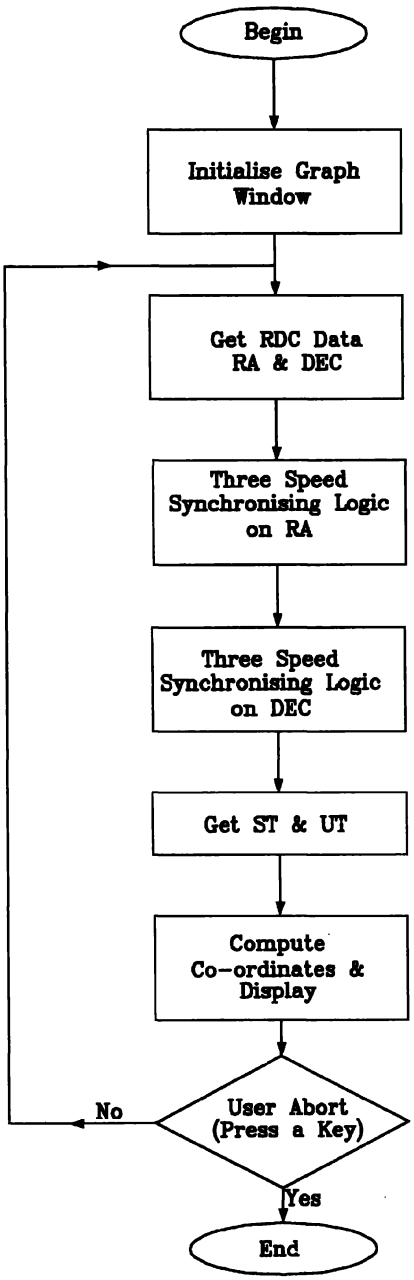

FIG. 4—Software flow chart.

"LstSec," "Lstfrac," "UtHrs," "UtMin," and "UtSec," returned by the procedure each time when it is called with the corresponding "Address," are used in the main program to obtain "ST" and "UT."

4.4 Compute Coordinates and Present to Graphic Display

Having obtained the position information of HA and DEC axes and the ST information, the coordinate RA is computed and hence the air mass and zenith distance can be evaluated using conventional formulas. The coordinates of star RA, DEC, the HA of telescope, ST, UT and the computed parameters air mass and zenith distance are all displayed on the monitor in graphics mode.

5. RESOLUTION AND ACCURACY

Resolution is enhanced in multispeed coarse/fine systems depending on the total gear ratio involved and the resolution of the fine converter. In this application, resolutions of 20 and 19 bits are obtained with a 12-bit converter on the fine shaft with the gear ratios of 1:24, 1:30, and 1:12, 1:30 for RA and DEC axes, respectively. However, the overall accuracy of the system depends on the accuracy of the fine synchro transmission, the gearing imperfections, and the accuracy of the fine converter.

The overall accuracy of the system can be approximated to be

$$G+I+(R+S)/N,$$

where, G=backlash and cyclic errors of spur gears, I=imperfections of the worm gear, R=accuracy of the fine converter, S=accuracy of the fine synchro, N=total gear ratio.

The backlash and cyclic errors of the spur gears should not be greater than the bit D of the coarse data for the given stage. The synchronizing logic corrects for the conflict in the readings that arises due to backlash and cyclic errors. So, the overall accuracy of the system depends on the accuracy of the fine synchro (S), the accuracy of the fine converter (R), and the gearing imperfections of the worm gear (I). For the AD2S80JD the accuracy is $\pm 8+1$ LSB arcmin. The accuracy of the fine synchro transmitter is ± 4 arcmin. Since the fine converter is configured for 12-bit resolution, the accuracy of the fine converter becomes $\pm(8+5.27)$ arcmin. Hence, the accuracy in the RA axis is $\sim 1.43+I$ arcsec ($N=720$), while for the DEC axis it is $2.86+I$ arcsec ($N=360$).

6. TESTING AND PERFORMANCE

6.1 Offset Adjustment

The electrical zero of a synchro is defined as the position where a maximum voltage is induced in S2 stator windings, i.e., when the rotor becomes parallel to the stator winding S2. The electrical zero of all the synchros needs to be offset properly in order to work with multispeed systems. In our system the software incorporates this feature. The offsets are found from the converter data when the telescope is parked in zero position. If the error in the offset plus the backlash error of a given stage is greater than the bit D (synchronizing logic section), then the synchronizing logic fails to correct the ambiguity in readings and a periodic jump in the readings occur.

6.2 Power Sequencer for RDC

The 2S80 series of the RDCs are susceptible to destructive latch-up when the +ve analog supply leads the −ve supply during power-up, causing excessive current from the +ve supply due to the parasitic transistors turn on. This destructive condition is eliminated by inclusion of a power sup-

ply sequencing circuit provided by Analog Devices (technical note on AD2S80, 1990). The power sequencing circuit ensures the +Vs is applied simultaneously or after −Vs supply.

6.3 Pointing Tests

After an initial offset adjustment, a more precise adjustment for the fine converter is obtained by reference to a known star position. Then the system was checked for other stars in the zenith region and repeatability tests were performed. The system has achieved a repeatability within ±1 LSB resolution. The data from the pointing tests using several stars are modeled using a pointing program resulting in a pointing accuracy of ±10 arcsec in RA and ±15 arcsec in DEC (both in rms) for any pointing of the telescope. The modeling program corrects for refraction and mount alignment errors.

7. SUMMARY

Replacing the synchro receivers with suitable electronics has offered a good solution in providing a digital-display system. The cost comparison favors this approach compared to the optical counterpart. This approach has also resulted in better reliability, resolution, and accuracy than the analog dial mode. Though the technique described above uses synchro and RDCs, it can be easily adopted to implement a high-resolution encoder using low-cost, low-resolution optical encoders in a gear train.

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REFERENCES

Boyes, G. S. 1980, Analog Devices-Synchro and Resolver Conversion

Data sheet of AD2S80 of Analog Devices 1990

Application software-passive component selection and dynamic modeling for the 2S80 series resolver-to-digital converters 1990

Technical note of Analog Devices- turn on and off sequencing for 2S80 1990