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Processing electronics instrumentation for the low energy detector of Solar X-ray Spectrometer (SOXS) experiment

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1. Introduction

Solar X-ray Spectrometer experiment is a joint program of the Tata Institute of Fundamental Research (TIFR), Mumbai, Physical Research Laboratory (PRL), Ahmedabad and Technical Physics Division (TPD), ISRO Satellite Centre (ISAC), Bangalore. It is proposed as a payload of opportunity on GSAT 2 to be launched in the year 2001. The main scientific objectives of this experiment are as follows :

(a) Study of X-ray emission during solar flares to understand processes leading to the acceleration of particles and subsequent energy release.

(b) Study of short term and long term variations of the solar corona.

The block schematic of SOXS experiment is shown in Fig. 1. SOXS experiment has two different detector **instrumentation** systems to study the low and high energy emission in X-rays. The low energy detector system consists of two detectors with built - in coolers namely, Si-PIN (to work in the range 4 – 20 keV) and Cadmium Zinc Telluride (CZT) (to work in the range 4 – 60 keV). The high energy detector system (SHD) consists of scintillation detectors that work in the energy of 15 to 3000 keV. The design details along with current status of Processing Electronics Instrumentation for the low energy detector system (SLE) will be discussed here. The details of the rest of the units in the SOXS instrumentatioon are not described here but are mentioned only for completeness.

The X-ray ban in the range 4 – 60 keV will be observed using these two detectors. The microprocessor (Inter 80C86) based processing electronic instrumentation system is designed to detect solar flares. The main function of the processor is to collect the data from Si-PIN and CZT at 100 ms integration time and check for flares by comparing with the pre-selected threshold. In the absence of a flare, the counter data is stored at 1 s integration. Once the flare is detected, it records the onboard time and acquires the count-rate and spectral data at 100 ms

resolution for 300 s. After 300 s, the spectral data is collected at 3 s resolution and count-rate at 1 s, for duration of 1800 s.The spacecraft being on a geostationary platform, the recorded data is transmitted to the ground station continuously at 12 kilo bits.s^{-1}.

2. Processing Electronics

A typical solar flare profile is shown in Fig. 2. The processing electronics for low energy detector instrumentation system is designed to fulfill the following major tasks.

a. Counting the events in the 4 energy bands namely, (5.5-6.5 keV), (10-13.5 keV), (13.5-14.5 keV) & (4.0-20 keV) in the case of Si-PIN and 5 energy bands, namely the above mentioned 4 bands + (20-60 keV) band, in the case of CZT detector and storing the data in SRAM.

b. Pulse Height Analysis (PHA) of events in the energy band (4-20 keV) in the case of Si-PIN and (4-60 keV) in the case of CZT detector, i.e., generating pulse height histograms of the events and storing the data in memory.

c. Detecting the solar flare by comparing the event counts with the pre-selected thresholds (threshold values are set by telecommand) and indicating to ground station through telemetry the flare status.

d. Digital data formatting and base band coding.

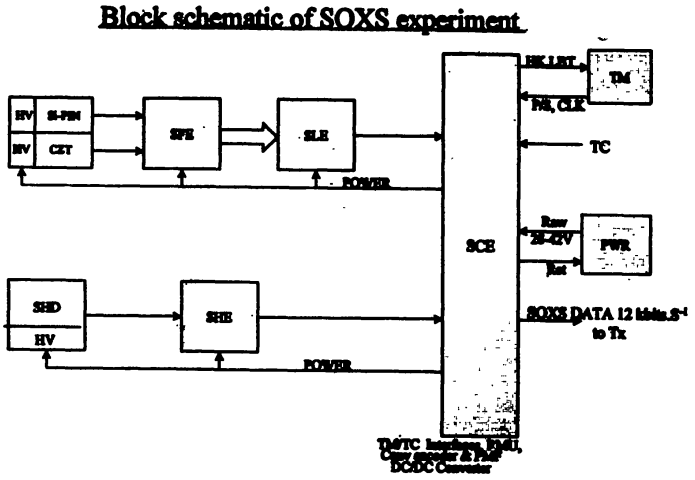
e. Playing back and transmitting the stored data to ground station on a continuous basis.

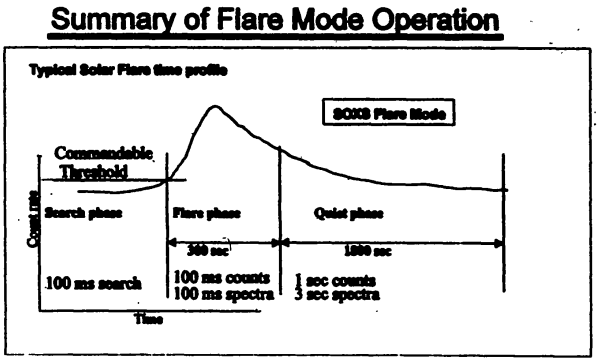
f. Flare detection information exchange with high energy detection system.

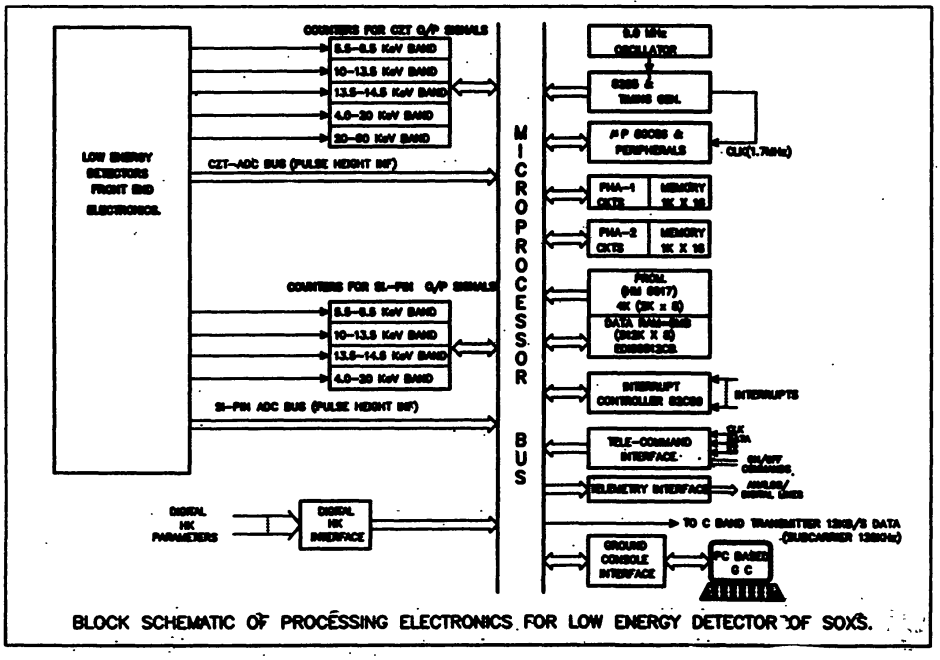
3. Design aspects of Low energy processing electronics

The block schematic of the processing electronics is shown in Fig. 3. The count rates to be handled by Low energy electronics are expected to be of the order of 40 kcounts. s^{-1} during flares (taking into account the geometry of the detector). Taking into consideration that the processor has to perform many functions (such as storing the 9 light curves at as fine as 100 ms resolution, storing the health parameters in memory and outputting the health parameters to telemetry etc.,) and the incoming events are random in nature, we have adopted an admixture of conventional hardware circuit and the microprocessor (intel 80C86 μP) based system to process the low energy signals. It is an interrupt driven system with a data memory of the size = 5.0M bytes. The instrumentation provides "a continuous data recording and playback". The system is designed with two banks of memory, each of size 2.5M bytes such that when one bank is acquiring the flare data over a 35 minutes duration, the other bank would be outputting the previously acquired data in this duration. Total memory is designed using 80 pages of 65, 536 bytes each (10 nos. of 512k x 8 MIL-STD SRAM manufactured by EDI, INC.,)

The system operates basically in three modes namely, Background, Flare, and Electronic Self Check modes. It has its interfaces through Common electronics packages (SCE) with the GSAT 2 spacecraft mainframe systems namely, Power (PWR), Telecommand (TC), Telemetry (TM) and Transmiter (Tx).







3. Status and future plans

The design, development, and testing of lab model of detector module, and front end electronics are completed at PRL and those of processing electronics module are completed at TPD, ISAC. The preliminary interface tests have been completed. The software design is in progress. Flight model of the system has been planned to be delivered by middle of the year 2001.