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Fast Photometry Using CCD

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Introduction

Observations of certain objects which exhibit fast changes in their light output seems to be of great interest in optical astronomy. Important informations can be obtained on their internal structures of the stars through the measurements of their pulsational frequencies. Long duration uninterrupted observations involving many observatories located at various longitudes on the globe have already been attempted in the case of white dwarfs and Ap stars, which have fundamental periods of 2 to 20 minutes, (Winget 1988). Pulsars have also evinced great interest which shows milliseconds to seconds periodicity in their radiation output. Such observations have been carried out using PMT as the detector (Santhanam et al. 1985). With the advent of solid state detectors like charge coupled devices (CCD) it is worth replacing the PMT with CCD for the following reasons. CCD has higher quantum efficiency (50%) as compared to PMT's (20%). CCD also provides a large dynamic range 10^4 than PMT and this factor is advantageous while measuring faint objects in the presence of bright ones. CCD's operate at manageable voltages ($\pm 15V$) and require no high voltages as demanded in the PMT operation. Though blue response of the CCD's lack compared to the PMT, this limitation has been overcome by coating the CCD surface with a wavelength shifter (Coronene) which gives an efficiency of about 15% in the range of $2000\ A^0 < \lambda < 4000 A^0$.

Technique and Hardware Description

The basic system comprises of a CCD detector (P8603 A, 576 x 385 pixels) at the focal plane of the telescope which receives the flux from the program object. In order to provide a fast readout, the object is imaged onto a window of 10 by 10 pixels on the right top corner of the CCD. Rest of the CCD regions are masked. For the image scale of 28 arcsec per mm at the Vainu Bappu Telescope prime focus, a good seeing image (1 arcsec) covers two pixels diameter. A larger window size has been provided to accommodate guiding errors and seeing quality changes.

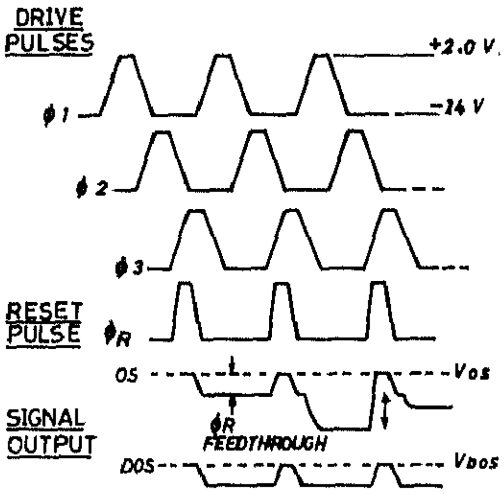

Figure 1. Drive pulse wave forms.

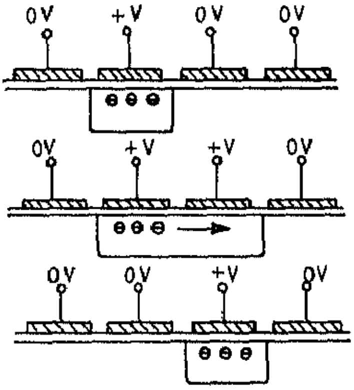

Figure 2. Charge transfer mechanism.

Since we are interested in the total flux output from the program object, the window region is combined to a super pixel by binning 10 rows into a single readout row and 10 coloumns into single serial readout pixel. Smearing of the image is avoided (to a large extent) by shifting the active rows much faster (4 micro seconds per row) compared to the integration time. The charge transfer mechanism is shown in Figs 3 and 4.

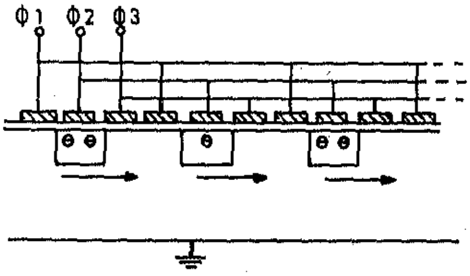

Figure 3. Charge movements with phases.

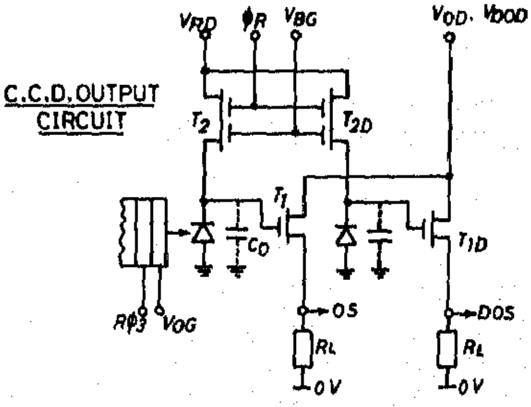

Figure 4. CCD output circuit.

Programmable Camera Controller

A hardware circuit has been designed to generate proper timing signal to allow integration time before shifting the active rows and coloumns into the readout pixel as shown in Fig.5. The integration period is programmable using thumb wheel switches (TWS) from 200 microseconds to seconds in steps of one microsecond. A 1 MHz clock advances a cascaded 9 stage decade counters. Coincidence is sought between the TWS and the counter values. This coincidence pulse clears the counters to start the next timing cycle. The coincidence pulse also triggers the row clocks $\phi_{H_1} - \phi_{H_3}$, ten times which provides binning of the rows. At the end of the row shift clocks, serial clocks $\phi_{V_1} - \phi_{V_3}$ as shown in Figs.1 & 2 are triggered ten times to allow for serial binning. The binning factor is programmable for varying window sizes.

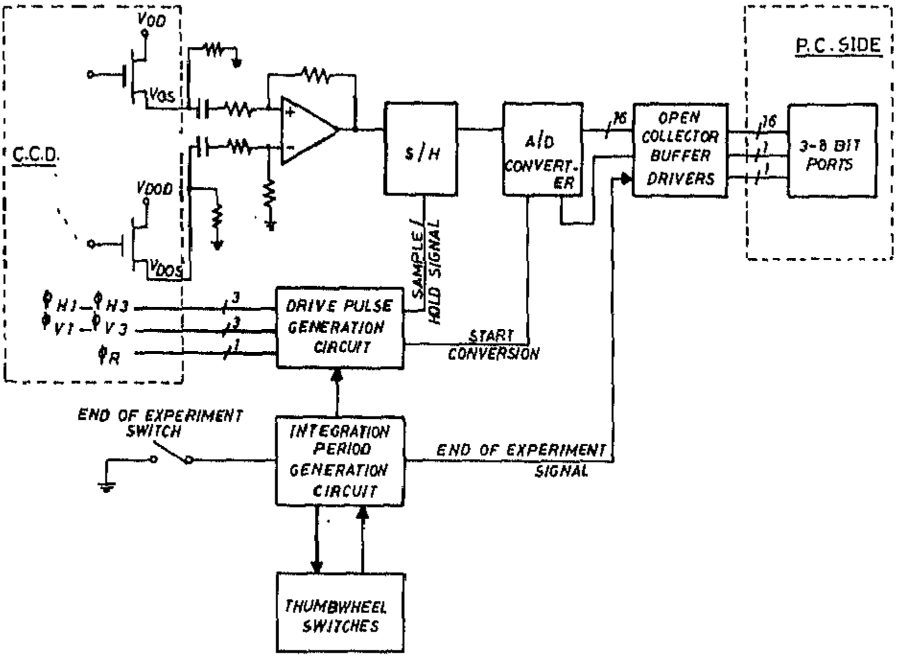

Figure 5. System hardware configuration.

Preamplifer and Analog to Digital Convertor

The charge detection amplifier consists of an output diode connected to a dual gate MOS transistor switch T1 and a second MOS transistor T2 operated in the source follower mode as shown in Fig.4. Prior to the charge output from the line readout section, T1 is switched by a reset pulse ϕ_R to precharge the output diode capacitance to V_{RD}. When ϕ_{V_3} goes low, charge under the last electrode is transferred to the output diode. There also exists a dummy output circuit which is arranged similar to the real output circuit but does not receive any signal charge. By employing a differential amplifier at the output as shown in Figs 1 & 5 any common signal like reset feedthrough and noise are rejected. OP-37 operational amplifiers are used in the preamplifier stage for low noise and high slew rate performance. The differential amplier output is routed to a high speed (16 microseconds conversion time) 16 bit analog to digital convertor (ADC AD 1376). A sample and hold circuit is employed to hold the analog signal steady during the ADC conversion. The 16 bit ADC output is interfaced to PC ports through buffers as shown in Fig.5. To match the input data rate with the storage in the hard disk, a double buffering scheme is used wherein the input data is dumped into one buffer, while the other buffer which has been filled with the previous data is routed onto the secondary storage.

Future Plans

Though the present technique is meant for studying a single star, it can be easily adapted to study more than one object by using suitable masks. The time series input data is proposed to be analysed using a two level reduction technique for period determination. At the first level, FFT technique shall be used to determine the approximate period, if any, in the data. At the second level, signal averaging is implemented on the input data using the approximate period information to build up the signal. The period which gives the best build up of the signal corresponds to the accurate period.

This is a proposed system and is under fabrication and testing. The results will be communicated later.

References

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