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Development of CCD camera systems at IIA

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Abstract. A complete CCD camera system consists of three modules: CCD dewar, camera electronics and acquisition software running on host computer. This paper describes the developmental activities going on in IIA towards a total camera system. The development of a three litre capacity liquid nitrogen CCD dewar is presented. An overview of a versatile CCD controller is also listed. An easy to use data acquisition software (DAS) developed under Microsoft Windows 3.1 is described. The DAS is modular and takes advantage of the Object Oriented features of Borland Pascal to provide custom specific tool boxes to implement various acquisition functions. The hierarchy of the software structure results in high flexibility to handle different CCDs.

Key words : CCDs-Dewar-Cryostat-CCD Controller-Data Acquisition Software

1. Introduction

Charge Coupled Devices (CCD) have become the choice of detectors in the field of astronomical imaging because of their high quantum efficiency, wide spectral response, linear response, large dynamic range, low noise, high geometrical stability and reproducible response. The high quantum efficiency enables imaging even fainter objects with moderate size optical telescope. The response spans a wide range of wavelengths (typically from 300nm to 1000nm) permitting various pass band photometric measurements. The linear response of the device provides a linear relationship between the observed quantities and the incident photons. The large well capacity (typically about 300K e- to 500K e-) with a low read-noise gives large dynamic range which allows imaging of both faint and bright objects in the same frame. Its high geometric stability and reproducible response gives stable performance over several years. However, CCDs need to be operated at lower temperatures (typically around –100 to –120° C) in order to reduce the dark current generation. Hence the device needs to be housed in a thermostat to achieve the cooling requirements that allow longer exposure times without any significant dark generation. The readnoise, which sets the final detection limit, can be reduced to few electrons by careful tuning of several parameters in the camera controller. A complete camera system for astronomical imaging would include a

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cooled CCD housed in a vacuum chamber, a camera electronics that manages the transfer of acquired image to the host computer and data acquisition software running on host to control the camera controller, to acquire the digitized data and to display/store the acquired frames. This paper presents the work being carried out towards a complete camera system for imaging with optical telescopes. The following sections present the details of cryogenicaly cooled CCD dewar, a flexible CCD controller and an easy to use CCD data acquisition software.

2. CCD dewar

The most common ways to cool the CCDs are either thermo-electric cooling (TE) or cryogenic cooling methods. The TE coolers are used for smaller detectors because of their limited heat pumping capacities. These are commonly employed in applications where input light flux is ample and hence exposure times can be shorter. TE coolers are sufficient to reduce the dark current generation to negligible levels when the CCD is operated in multi-phase pinned (MPP) operation. Multistage TE coolers allow to reach temperatures of -100° C where CCDs in normal operation can be used. The cryogenically cooled dewars are designed (Luppino etal., 1992) to operate the CCDs at well below -100° C. Such a dewar would include a liquid nitrogen container with fill and vent structures housed in a vacuum enclosure. In either case, the CCD is mounted inside the vacuum chamber and the mount is connected to the cold surface within the dewar. The input light flux enters through an optical window and made incident on the CCD. The electrical signals are connected through a vacuum sealed connector. The following section describes a liquid nitrogen cooled CCD dewar design that is being developed.

2.1 LN_2 chamber and camera head

The dewar consists of two parts; one is the LN_2 chamber housing and other is the CCD camera head. The chamber housing encloses a three litre capacity liquid nitrogen container, molecular sieve, fill & vent structure and a vacuum port. The CCD camera head contains a CCD mount, an optical window and hermetically sealed connector for electrical signals feed through. The cold connection to the CCD mount is established through a pair of copper straps held by a compressible spring. The CCD mount also contains a resister heater and temperature sensor. The two parts are vacuum sealed by an O-ring and can be easily separated without any internal disconnection to the cold connection. The LN_2 container is connected to the back plate through a thin tube (neck tube) with a wall thickness of about 200μ. The neck tube is welded to a holder that connects to the back plate of the body through an O-ring assembly. The LN_2 container is firmly fixed to the outer jacket through three Teflon washers at each 120° apart. The outer body of the camera head is made in octagonal shape that allows easy mounting of the vacuum sealed electrical connectors. The lower and upper portions of the vacuum jacket are also matched to the camera head. An assembly sketch of the dewar is shown in Fig.1. The dewar is undergoing some modifications and hence further details are not available. They will be made available once it is perfected.

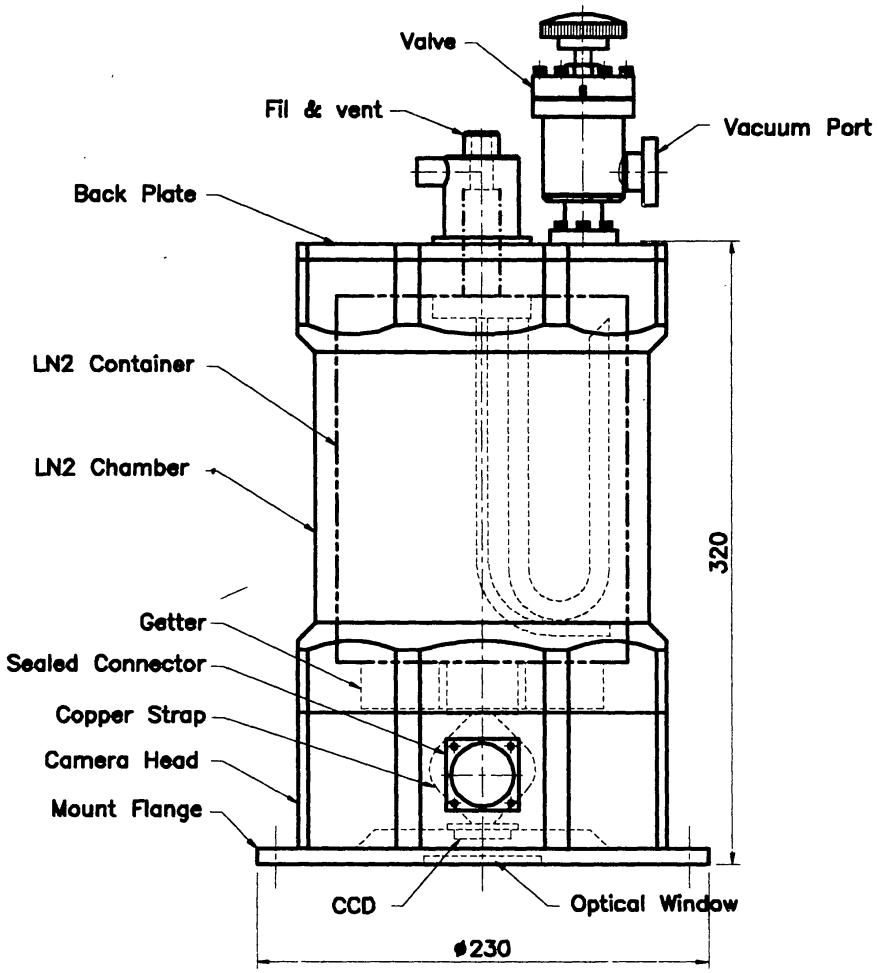

Figure 1. CCD dewar assembly

3. CCD controller

3.1 General objectives

A CCD controller should give an optimum performance when imaging with scientific CCDs. There are several subtleties in achieving an optimum performance. 1) The charge transfer should be properly done to ensure the device's charge transfer efficiency (CTE) performance. Normally, the CTE of a CCD is optimized by applying proper bias voltages, clock levels and clock sequence. 2) The controller should operate at a fast rate to improve the observing efficiency. 3) Window

and binning readout should be possible in order to have a fast field preview and focusing. This helps in quick determinations of observing parameters to be made at the site. 4). A new generation controller would incorporate various features to operate different format CCDs from different manufacturers. 5) The controller should be stable; drift in the offset over time should be as minimum as possible. 6) The controller is expected to be compact so that it does not occupy much space and a less heat dissipative so that it does not disturb the thermal environment at the telescope, and 7) The controller should be flexible to program for various modes of operation like window readout, binning the pixels, time delay integration etc. Recently, a controller that meets nearly all these requirements, has been developed at this institute. The following section presents a description and the capabilities of this general purpose controller.

3.2 Overview of Universal CCD controller

The basic timing generation is implemented with a set of EPROMs which derive their address lines from set of asynchronous counters running at 1 MHz. The required parallel, serial and binning wave forms are stored in the EPROMs at different locations. The controller supports window readout and binning pixels. The controller incorporates Digital to Analog Converters (DAC) to set the bias and the clock levels. This adds to the programmability in optimising the CTE performance of the device. The controller operates at 40 KHz that takes about half a minute for 1k * 1k readout. It is capable of operating a single readout, 4 phase CCDs. It interfaces with the host computer on a parallel port and thus, flexible in programming for various modes of operation. The other specifications are that the board is a six-layer PCB measuring less than A4 size-occupying less space. Laboratory tests are favouring to stable performance. The following section describes the various building blocks of the controller.

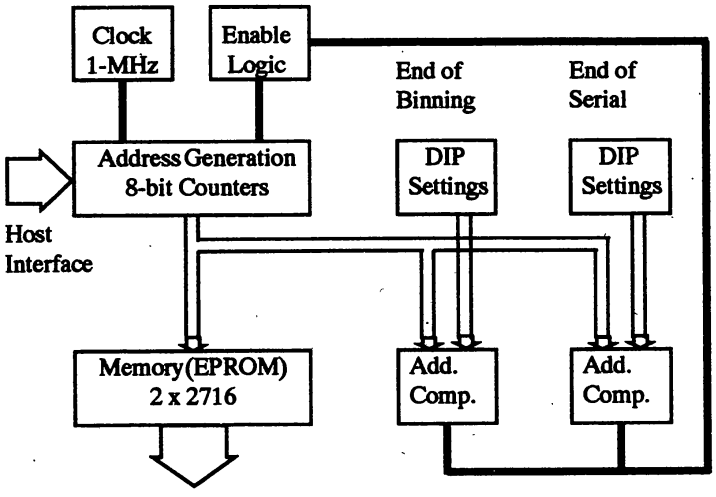

Figure 2. Block diagram of waveform sequencer.

4. Building blocks of controller

4.1 Waveform sequencer

The function of the waveform sequencer is to define the level of the various clocks and other control signals at a given instant. The clocks include serial clocks, parallel clocks and a reset gate. These are required for proper charge transfer from image area to readout register and then to the output amplifier. The control signals include integrate reference, integrate signal, reset integrator, start ADC conversion etc. These are required for processing and digitizing the signal from CCD. The timing waveforms are encoded as states and are stored in successive memory locations in a set of EPROMs. These locations are accessed one after another to generate the required timing pattern. The EPROMs derive their address from a set of counters which can be programmed by the host. So, depending on the type of the waveform that needs to be generated, the host loads the counters with the corresponding starting address of the waveform. A block diagram of the waveform generator is shown in Fig.2.

4.2 Clock generation and bias voltages

CCDs require different clock levels for proper charge transfer. Two 12-bit DACs followed by buffers with suitable gains are used to set the ON and OFF levels of a required clock. A high speed analog switch selects these levels to the output depending on the level (1 or 0) of the state bit derived from the waveform sequencer. A passive RC filter at the output of the analog switch provides clock edge shaping. This also acts as RFI filter immediately before the dewar and to minimize the interclock cross-talk. Various bias voltages such as reset drain, output drain, are generated using 12-bit DACs followed by suitable gain amplifiers. All the bias supplies can be enabled or disabled remotely. The logic ensures that the bias voltages are not applied to CCD immediately after power-on.

4.3 Signal processing

4.3.1 Signal coupling and pre-amplifier

The signal processing chain includes DC offset removal, pre-amplification, double correlated sampling, bias offset and digitizing the signal. The CCD source follower load provides a constant current source. The signal is capacitively coupled to the pre-amplifier to remove a constant DC offset in the signal. The inherent advantage of this AC coupling is that the signal is immune to the bias voltage and temperature drifts. The preamplifier amplifies the CCD signal and is configured with selectable gains for selecting the dynamic range of the system (e- / ADU). The block diagram of the signal processing chain is shown in Fig.3.

4.3.2 Reset noise - Double Correlated Sampling

To measure the charge collected under each pixel, the output capacitor is pre-charged to a reference voltage by turning on the reset transistor. The thermal agitation of electrons in the reset transistor causes certain amount of uncertainty in the mean value of the final reset voltage on the capacitor. This uncertainty in the final voltage is called reset noise and is given by Reset noise = $\sqrt{(kT/C)}$

Volts where k is the Boltzman constant, T is absolute temperature and C is the node capacitance. Usually, this noise exceeds the output amplifier noise. The double correlated sampling (DCS) technique eliminates this reset noise by taking two samples of the CCD signal per pixel, one before and one after the charge packet is shifted to the node capacitor. The reference signal is positively integrated over a defined period of time and after the charge shift, the signal is negatively integrated for the same amount of time. The resulted output at the integrator is proportional to the detected signal and is free from the reset noise.

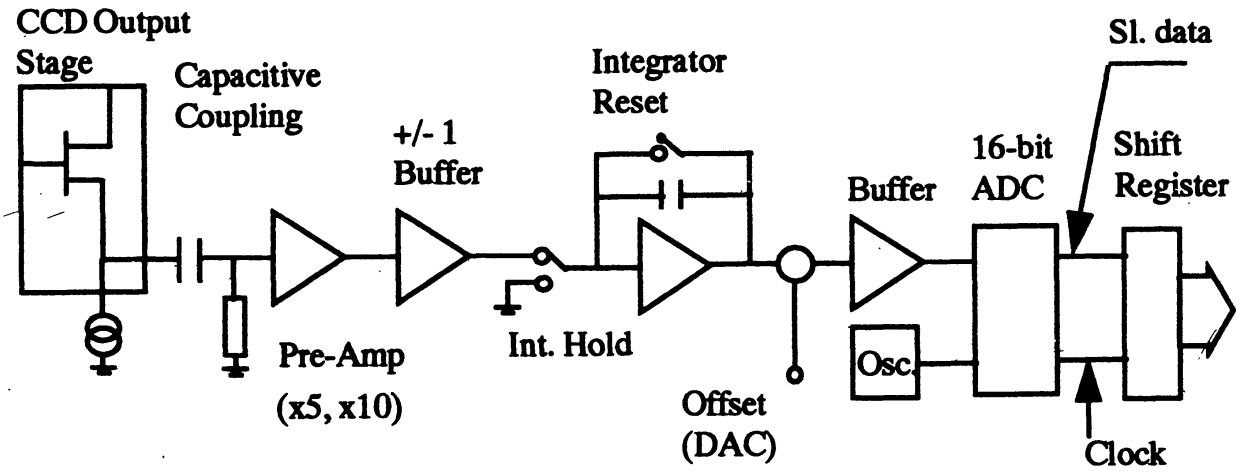

Figure 3. Block Diagram of Signal Processing Chain

4.3.3 Offset buffer and ADC

A buffer preceeding analog to digital converter (ADC) presents a low impedance to the sample and hold of the ADC. An offset signal can be added to avoid clipping at ADC input. The ADC buffer also isolates the integrator from the ADC to avoid feedback to the former. An anti-aliasing filter following the buffer ensures that the ADC does not see any high frequency noise caused by the buffer. A 16 bit ADC - CS5101A (Crystal, 1992) - is used to digitize the processed signal. The CS5101A consists of two channel multiplexer and a sampling device. The conversion time is 8 uS and the digitized data is output in serial form. Auto-zeroing capability of the device enhances power supply rejection at frequencies well below the conversion rate. The ADC is configured in unipolar mode and code output is in binary format with a range of 0 to 65535. The serial data is then converted into 16 bit parallel data by a set of shift registers.

4.4 Host interface

The controller interfaces with the host on a 16 bit parallel input / output port of an ISA bus. The ISA interface board consists of address decoder, a command port and data port. The command / data lines are sent / received through differential line drivers / receivers. The 16-bit digitized data is read by the host a byte at a time. There is no-on board memory in the controller and hence the host is dedicated to the in coming data stream during readout.

4.5 Utility functions

The controller is integrated with a temperature control circuitry. The desired temperature in the CCD dewar can be set on the dial on the front panel. When the dewar is filled with LN_2 the CCD mount is heated to the set temperature and stabilizes at the set point. The CCD mount temperature is indicated on the front panel in Kelvin. The temperature display can be switched on or off remotely by the host. Shutter controls are provided to control the exposure times.

5. CCD data acquisition software

The CCD data acquisition software has undergone rapid developments with the advent of the high-tech computer hardware, operating systems and various compiler technologies. The Microsoft Windows has provided the user with a graphical interface - a screen display in which the user issues the commands by pointing and clicking the on screen elements. It also provides a complete operating environment in which an application program can run offering features that are not available in MS-DOS. Both the user and the programmer are benefited in the windows environment. The user gets advantages such as multitasking, inter-application cooperation and drivers to support several peripherals. The programmer is relieved from writing code specific to the output device by the windows graphics device interface (GDI) unit. The event-driven architecture generates messages on an input event and the messages are placed in a queue for the appropriate application program. So, no need for the code that loops indefinitely waiting for an input event. The programmer need not bother about memory allocation / reallocation as needed under multi-tasking environment. Windows takes care of all these for each application through its memory manager using handles. Windows provides facility to maintain the resources outside the programs source code and allow the use of the dynamic link libraries. However, programming for window environment demands an in-depth knowledge of events, formats, handles and inner workings. Object-oriented approach simplifies the task of programming for windows by using objects which manage the message-processing behavior and insulate the developer from the details of inner workings of windows. As a result, a window application can be developed in much less time and effort compared to conventional approaches. We have developed an easy-to-use CCD data acquisition software using the Object Oriented Programming approach for MS-Windows 3.1 using Object-Pascal for windows. The hierarchy and the functions of the acquisition software are described in detail elsewhere (Nagaraja Naidu et al., 1997). For completeness, the following section summarises the functionality of the software.

5.1 Functions of software

The acquisition software is broadly divided into i) CCD camera related controls, ii) image acquisition and display functions, iii) analysis and utility tools. The camera related functions allow control over setting up the camera parameters, setting of bias and clock levels, readout controls etc.. The acquisition performs acquiring bias, dark and image frames. These also include acquisition of a window region or focus mode of operation. The display functions provide various ways of looking at the stored / acquired data. They include zoom, squeeze and pan. These methods include various data scaling and intensity mapping methods. The scaling methods include i) dynamic min. / max., ii) fixed min. / max. and iii) histogram equalisation methods. The intensity mapping functions include i) linear ii) logarithmic iii) binary methods and iv) pseudo-color mappings. Analysis functions include graphical representation of data such as row, column and histogram plots. Basic image statistics like image min. image max and standard deviation are included in the analysis functions. An utility to evaluate the camera system gain and on-line help are provided.

6. Put together

The data acquisition software is integrated with the hardware settings of the CCD controller as needed for an EEV P8603 CCD. The laboratory experiments showed satisfactory performance. The software flow for a full frame readout is as follows.

6.1 Sequence of charge shifting

After the exposure is completed, the counters are reset and enabled which initiate a parallel transfer. The end of the parallel transfer is indicated by a status bit in the host interface board. When the status bit sets, the program clears it, and the counters are loaded with the serial shift starting address (in EPROM). After every single serial shift (single pixel) the counters are automatically loaded back with the starting address and the process continues indefinitely. After every pixel is digitized, the end-of-conversion pulse from ADC sets the status bit. Then, the digitized data is read in two bytes into the host and the status bit is cleared. Once the serial registered is read, the program resets the counters to cause another parallel transfer and the process is repeated for the desired number of parallel transfers.

6.2 Software flow

The CCD controller is configured and loaded with the proper bias and clock levels using the select CCD dialog box and 'Camera Reset' command. A new image is created which allocates sufficient memory for data and bitmap. After the exposure, the charge is shifted and digitized as described above. The digitized data is transferred to the global memory for every parallel transfer. At the end of the parallel register readout, a bitmap record is created from the acquired data and is displayed in the image window. The image header record is then updated and attached with the acquired image.

7. Conclusion

Three developmental activities are described. The CCD dewar being developed is outlined with its features though full details are not possible at this stage. The building blocks of a general purpose CCD controller are presented. The functions of an easy-to-use CCD data acquisition software developed for MS Windows are briefly described. Finally, integration of the software with the hardware as applicable to EEV P8603 is described.

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