Bull. Astr. Soc. India (2002) 30, 215–221

Signal Processing Instrumentation of Gamma - Ray Telescopes of the GRACE Project

P.K.Mukhopadhyay

Electronics Division, Bhabha Atomic Research centre, Trombay, Mumbai – 400 085, India

Abstract. The TACTIC Cerenkov telescope has recently been commissioned at Mount Abu, Rajasthan. The signal processing electronics of the 349 element imaging camera was a totally indigenous development. A number of groups from Electronics Division and NRL, BARC participated in the development of the various subsystems of the imaging camera which included multichannel detector bias supply, fast amplifier, charge to digital converter, 50MHz scaler, programmable trigger generator and data acquisition electronics. Most of the multichannel electronic modules followed either the NIM or the CAMAC standard. A considerable amount of interconnection cabling was necessary. In the second phase of GRACE project two further telescopes, namely MACE and MYSTIQUE have been proposed, each having a considerably larger number of channels. Implementation of these projects with the existing type of instrumentation would pose formidable problems of interconnection, testing and maintenance. A new type of integrated module has therefore been proposed. Each of these modules would provide sixteen channels of pulse processing electronics, first level trigger generation and an onboard data acquisition and communication processor. These processors would be networked by ethernet interface. Similarly, detector bias would be generated with sixteen channel HV modules with onboard processors, which would also be networked with a slower link. This type of high density pulse processing electronics would significantly reduce the interconnection and maintenance problems. However the required high density electronics is achievable only with extensive use of hybrids and ASICS. Work has been initiated for fabrication of fast amplifiers in hybrid form. Similarly, multichannel scalers and constant fraction discriminators would be implemented in ASIC.

1. Introduction

The Bhabha Atomic Research Centre (BARC) initiated a program to build a ground - based gamma - ray ast telescope array called TACTIC (TeV Atmospheric Cerenkov Telescope with Imaging Camera) in the VIIIth 5-year plan. The effort was rewarded with the observation of variable emission from the extra-galactic source Mkn-501 with the partially completed TACTIC telescope in the year 1997 (Bhat et al.,1997). The telescope has been completed recently and is ready for regular observations. The commissioning of the TACTIC is a significant achievement for Indian science and technology. The design and fabrication of the telescope and its instrumentation was a totally indigenous effort. In the IXth 5-year plan, BARC initiated programs for fabrication of two even more complex gamma ray astronomy telescopes (Bhat, 2000) , namely MACE (Major Atmospheric Cerenkov Experiments) and MYSTIQUE (Multi-Element Ultra-Sensitive Telescope for Quanta of Ultra-High Energies) which place even more stringent requirements on instrumentation.

2. Pulse processing instrumentation of TACTIC telescope

The TACTIC telescope array has a central imaging telescope at the centroid of three vertex element telescopes forming an equilateral triangle of 20m side. The central telescope has a 349-pixel imaging camera at its focal plane while each vertex element deploys a 58-pixel duplex camera (Tickoo et al., 1999). The block diagram of TACTIC pulse processing instrumentation is shown in Fig-1. Each pixel detector in the TACTIC is a PMT powered by its own dedicated channel of computer controlled HV supply. When gamma induced Cerenkov photons are incident, the PMTs generate fast pulses at the anode. These pulses are

amplified by the fast amplifier channels (Joshi and Mukhopadhay, 1995). The amplifier outputs are used to derive timing signals as well as charge content information for imaging the celestial gamma source.The timing signals are derived from the amplified fast pulses with leading edge discriminators. These, in turn are input to a memory - based reconfigurable fast coincidence unit (Kaul et al., 2001). When coincidence conditions are satisfied, a gate signal is generated to enable the charge to digital converters (CDC) in all the channels (Vaidya et al., 1997). Since there is a substantial delay from timing signal to the CDC gate signal, an appropriate equalising cable delay is introduced in the analog signal input path to each CDC. The charge information from the CDC and the event time information from the clock are stored by a data acquisition computer.The discriminator timing signals are also counted by the channel scalars to monitor and control the singles event rate of the channels. Corrective action is taken by adjusting the computer controlled high voltage channels to keep the count rates within 10 to 15 kHz.

The HV system (Manna et al.,1993) is built up of modules, each of which has eight independent HV channels. Ten such modules are housed in a custom built crate that also houses a crate controller and the power supply. The crate controller provides the computer interface for controlling and reading the high voltages. All such crates are controlled by a single computer (node-3) .The fast amplifiers and the leading edge discriminators are NIM modules while the CDC, scalers and the memory based coincidence units are CAMAC modules. The crates are controlled by CC-7 crate controllers(Arvindakshan et al.,1993). These are in turn controlled by the data acquisition computer (node-1). Thhe data acquisition computer and the HV control computer are in turn controlled by a master node computer (node-2).

Table 1: Modular instrumentation for TACTIC imaging

Module	Standard	Channel per module	Total modules	Salient specifications	Design group
1.HV	PROPRIETARY	8	68	0 to -2.5KV, 2ma max., overload protected, computer controlled	ED/SPL
2.Fast amplifier	NIM	6	90	Gain: variable up to 50 Transition time : <3ns	ED/NIM
3. Leading edge discriminator	NIM	4	136	Threshold: 0 to –2.5V	ED/NIM
4. CDC	CAMAC	8	68	F.S. : 600pC	ED/NIS
5.Scaler	CAMAC	6	90	Max freq.: 50MHz	ED/DAPS
6. CAMAC crate and CC7 crate controller	CAMAC		16		ED/DAPS
7.Trigger generator	CAMAC		7		NRL
8. Delay generator	CAMAC		1		NRL
9. Fan-out module	CAMAC		10		NRL
10. Event handler	PC-CARD		2		NRL
11.Precision μs timing system			2		NRL

3. The proposed GRACE Instrumentation Module

The proposed new telescope MACE would employ 832 pixel camera in the focal plane of a paraboloid reflector. The instrumentation for the pixels would be housed in an enclosure supported from the frame of the telescope imposing weight and space constraints. The MYSTIQUE telescope would employ 1024 pixels distributed over a large area.. In the light of experience gained with the TACTIC instrumentation, a review of the suitability of the old instrumentation was in order. The following limitations were apparent.

a. Each pixel instrumentation channel requires five cables, each of which requires two connector pairs.

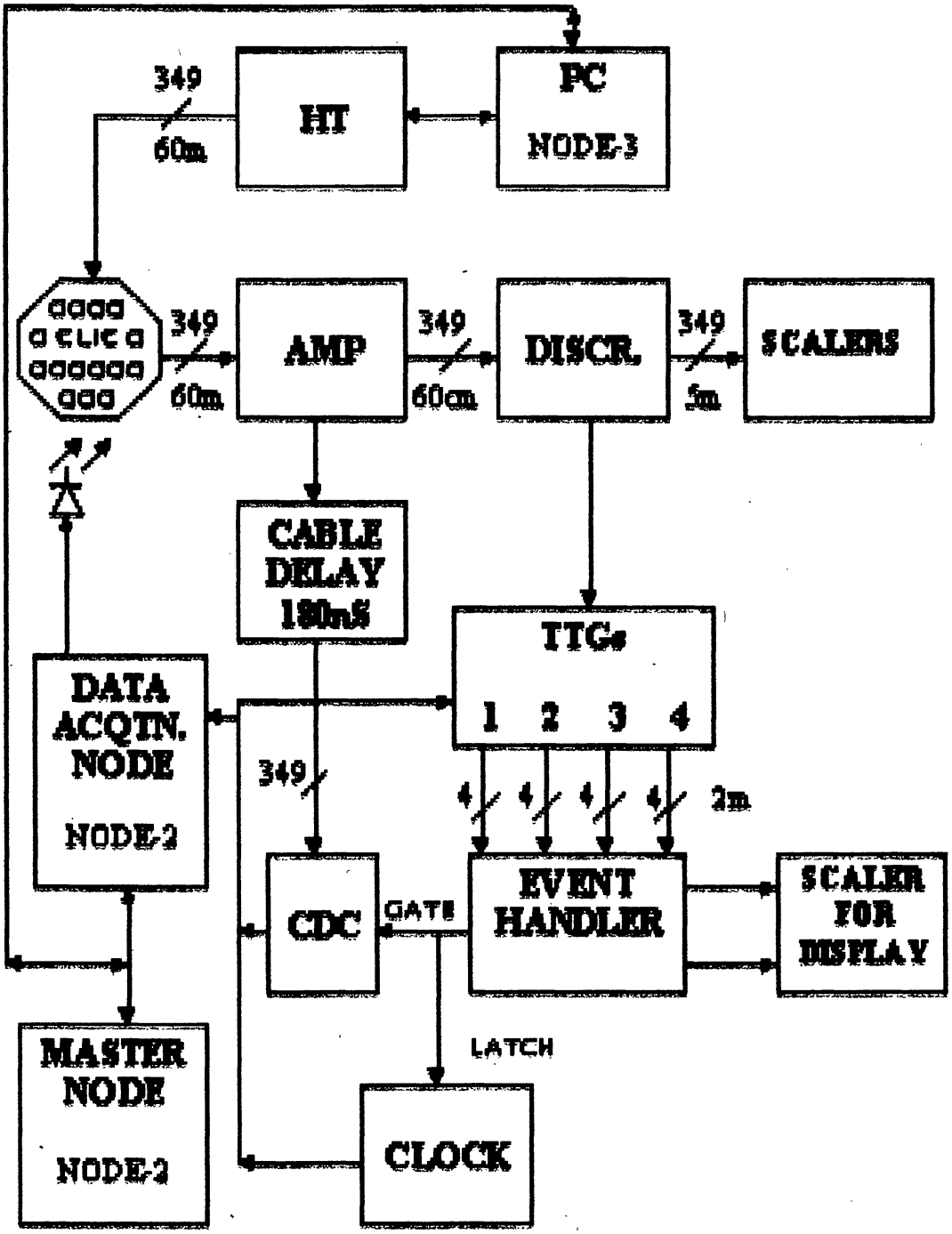

FIG.-1: TACTIC IE BLOCK DIAGRAM

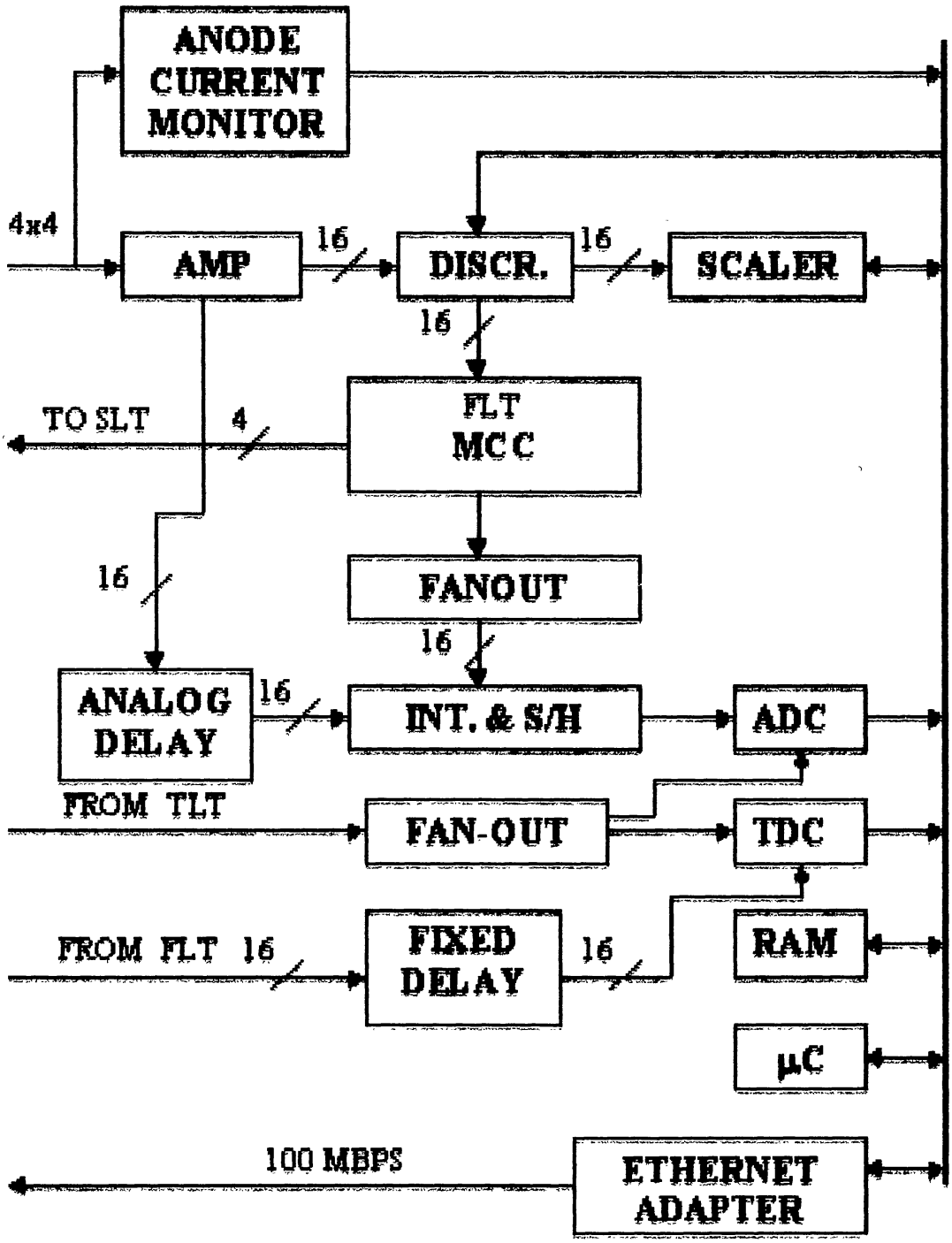

FIG.-2: BLOCK DIAGRAM OF GEM

b. The delays in the PMT signals have to be equalised manually by adjusting cable lengths in each channel.
c. The TACTIC trigger generator provides gate signals to the CDCs after comparing trigger signals from all the channels. This process takes time so that the signal to the CDC has to be delayed by 180ns . Since lumped delays of this magnitude would spoil the shape of the fast rising signals, delay cables are used which, nevertheless, degrades the signal to some extent. Because of this and the scatter involved in delays of several cables, the CDC gate width is kept at 40ns with attendant increase in step noise even though the basic pulse width is only 15ns.
d. The old instrumentation consumes a large amount of power and would be disadvantageous particularly for the MACE telescope where the entire instrumentation is to be mounted in a small enclosure below the telescope frame.

In view of the shortcomings of the old instrumentation, a new scheme has been proposed (Working Group for GRACE Electronics, 1999). This scheme eliminates a major part of the interconnections by integrating the signal processing electronics of sixteen channels in a single module named as GEM (GRACE Electronic Module). The detectors are arranged in basic blocks of sixteen in these experiments. One such module would process the signals from one such block. The design objectives of the new instrumentation are as follows.

a.Manual delay adjustment would be eliminated by provision of electronic delay adjustment of the discriminator output.
b.The large analog delay in the CDC input signal would be eliminated by use of gate signal generated from local coincidence. The CDC data would be accepted when global coincidence conditions are met.
c.Space, weight and power requirement would be minimised by use of hybrid microcircuits and ASICs where necessary.

The block diagram of the GEM is shown in Fig-2. The module would amplify the analog signal from each channel and derive timing signal from them. These would then be used to derive a first level trigger (FLT) on board with small time delay. The FLTs would activate the charge integrator and the sample and hold circuit following it. The analog delay necessary in the CDC input signal path would be about 30ns, which would be significantly lower compared to 180ns in the old scheme. Since the interconnection delay from timing signal to trigger generator would be very small, and any residual delay mismatch would be electronically tuned out, a smaller coincidence interval can be used, which would lead to reduction of random coincidence rate. Further, step noise in the CDC output would be reduced by use of a smaller integration interval which would be feasible due to reduction of timing delay mismatch.The FLT of various neighbouring modules would be used to derive a second level trigger (SLT). The SLTs would in turn be combined to form a third level trigger which would initiate charge digitisation in the CDCs followed by capture of data from the CDCs and the event time from the clock. The arrangement is shown in Fig.3. As in the case of TACTIC instrumentation, the coincidence logic would be fast memory based and therefore reconfigurable. Internal control as well as data transfer between the module and the data acquisition computer would be effected by an onboard SBC.

The GRACE Electronics Module would have the following subsystems:
Photomultiplier anode current monitor
Pulse amplifier
Constant fraction discriminator
Scaler
First level trigger
Charge to digital converter
Time to digital converter
Memory for data storage
Single board computer (SBC) for control and ethernet interface

The functional description of the various subsystems is as follows:

Anode current monitor: This is a DC measurement circuit for monitoring photomultipler anode current. The digitised output would be interfaced to the SBC bus. The maximum rated anode current of the photomultipliers is 200 microamps. However, to ensure safety, they would be operated in the range 10 to 20 microamps and the current would be continuously monitored. In the event of excursion above this limit the high voltage would be lowered to reduce the current.

Pulse amplifier : This is a two-stage pulse amplifier with adjustable gain up to 100 and rise time of about 2ns. This would amplify the negative fast pulses from the PMT anodes. Each amplifier stage would be a hybrid microcircuit (Chandratre et al., 2001) .

Constant fraction discriminator: The electronic circuitry of the CFD would be fabricated as an ASIC (Shrivastava et al., 2001) .This would provide a timing signal if the input pulse amplitude exceeds a programmed threshold. The output would be nominally free from timing walk due to amplitude variation. A timing signal with programmable delay would also be available. Thus it would be possible to equalise channel delays for the purpose of coincidence timing.

Scaler : This would be fabricated as an ASIC. This would provide a 32-bit timer and sixteen 32-bit scalers so that only one IC would be necessary for one module. This would be interfaced to the SBC bus. This would be used for continuous monitoring of count rate of each channel for taking corrective action by change of high voltage if necessary.

First level trigger : This would be a fast RAM based coincidence generator for deriving a FLT. Using a RAM with 16 address and 4 data lines, four different trigger types can be generated simultaneously. The coincidence input pattern can be programmed with the onboard SBC. The FLTs from neighbouring modules would be used to derive a SLT.

Charge to Digital Converter (CDC) : The FLT would trigger the charge integration process with appropriately delayed output pulse from the fast amplifier as input. The charge value held in the sample-hold circuit would be digitised at the occurrence of TLT within a specified duration after FLT. An improved version of CDC is currently under development (Vaidya et al.,2001).

Time to Digital Converter : This is a single start multiple stop time digitizer with full scale range of 500ns and resolution of 0.5ns. It would be used to measured time interval between the TLT and the FLTs , the TLT would be used as start and appropriately delayed FLTs as stop.

Memory : This would be used for temporary storage of CDC and TDC data before final storage in SBC memory.

SBC : This would be a 486 or higher processor based SBC with sufficient flash ROM and normal RAM to accommodate the necessary operating software. It would also have a built-in ethernet interface for communication with the master computer.

4.Development of Hybrid Microcircuits and ASICs for GEM

4.1 Counter-timer ASIC

A counter-timer ASIC with 16 counters, capable of operating at high count rate, has been proposed. It would be implemented with the 1.2 micron CMOS technology available at ITI, Bangalore. The ASIC would find use in other experiments involving simultaneous multichannel counting. The principal features of this ASIC are as follows:

16 counters of 32 bits each
1 timer of 32 bits with 16-bit prescaler (for prolonged counting with fast clock) and preset time register
Software and hardware reset
Data read on the fly capability for counters as well as the timer
Testability of all counters and the timer
PC compatible 8 bit I/O bus

4.2 Constant fraction discriminator

In the first phase of TACTIC instrumentation, leading edge discriminators were used to derive timing information from the detector pulses. These discriminators are relatively simple in construction but suffer from amplitude dependent timing walk, which leads to timing uncertainty. In the first phase instrumentation this was tolerable since the time gate interval for coincidence was relatively large. In the second phase instrumentation this interval would be smaller to reduce random coincidence rate. In this case the same walk would be a larger fraction of gate width. So it was decided to use constant fraction discriminators (CFD) for deriving timing information. This type of discriminator has better walk characteristics. However the circuitry is more complex and expensive.

In TACTIC instrumentation the delays between different channels were equalised by adjusting cable lengths. This method would be inapplicable in case of the new instrumentation in view of the larger number of channels and more stringent accuracy requirement. A method of electronic adjustment of delays would be more desirable.The requirement of extra functional complexity with increased packaging density can best be met in an ASIC implementation of the CFD circuitry. An ASIC design incorporating a CFD and an adjustable delay has been developed and simulated (Shrivastava et al., 2001). The fast bipolar transistors to be used in this design will be fabricated by a process developed at IIT Kharagpur. The block diagram of the ASIC is shown in Fig.4.

4.3 Fast hybrid amplifier

In the first phase of GRACE instrumentation, the fast amplifiers were constructed as NIM standard quad amplifier modules with gain of 50. Each channel of the amplifier consisted of two fast amplifier circuit blocks built with standard components. For the GEM modules the fast amplifiers will be realised with hybrid fast amplifier building blocks. They provide amplification of 10 in the output range 0 to –2.5V with 50 ohm drive capability. The performance of these hybrid amplifiers would be similar to that of Lecroy VB100 amplifiers. These are therefore likely to be used in other applications requiring fast pulse amplification

5. Programmable multichannel high voltage

A 16 channel high voltage module is under development (Manna et. al., 2001). Each channel would provide 1mA at 2KV. Each is independently programmable through on-board microcontroller which communicates with external computers through a serial I^2C bus as well as through RS232-C link. The individual supply voltages may be read back. Each supply is overcurrent protected. The size of the converters has been reduced by employing a higher operating frequency as compared to the HV system in TACTIC instrumentation.
The interconnection of the system consisting of the HV-system, the GEM modules and the programmable coincidence unit along with the controlling computer is shown in Fig.5.

6.Conclusions

The requirement of large amount of instrumentation for TACTIC provided learning opportunities and challenges for the nuclear instrument designers of BARC. Much of the instrumentation developed is versatile and may be used in other physics experiments. The requirement of larger scale instrumentation for MACE and MYSTIQUE telescopes has underlined the need of miniaturisation thus giving a fillip to hybrid microcircuit and ASIC design activities. The fast amplifier, CFD, counter-timer and CDC are likely to find wide use in future nuclear instrumentation work.