Mosaic CCD camera system: Implementation and application to astronomical imaging

A thesis
submitted for the degree of
DOCTOR OF PHILOSOPHY

In
The Faculty of Science
Bangalore University, Bangalore

By
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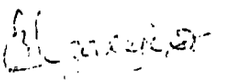
August 2001

Declaration

I here by declare that this thesis is the result of the work and investigations carried out by me at the Indian Institute of Astrophysics, Bangalore under the supervision of Prof. R. Srinivasan and Prof. Ram Sagar. This thesis has not been submitted for the award of any degree, diploma, associateship, fellowship etc. of any University or Institute.



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Certificate

This is to certify that the thesis entitled "Mosaic CCD camera system: Implementation and application to astronomical imaging" submitted to the Bangalore University by Mr. B. Nagaraja Naidu for the award of the degree of Doctor of Philosophy in the faculty of Science, is based on the results of the work and investigations carried out by him under our supervision and guidance, at the Indian Institute of Astrophysics. This thesis has not been submitted for the award of any degree, diploma, associateship, fellowship, etc. of any University or Institute.

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Acknowledgements

It is my pleasure to thank my thesis supervisors, Prof. R. Srinivasan and Prof. Ram Sagar. I am grateful to Prof. Srinivasan for his guidance and keen interest shown throughout this thesis work in spite of his busy schedules. I am indebted to Prof. Ram Sagar for all his encouragement and guidance during observations and data reductions. I thank Prof. R. Cowsik, Director of the Indian Institute of Astrophysics, for providing all the facilities to build CCD camera systems in house.

I would like to thank the Chairman of the Physics department, Bangalore University, Prof. M. N. Anandaram, the former Chairmen Prof. A. R. Hanumanthappa, M. C. Radhakrishna, and the faculty of the Bangalore University for their cooperation from registration to till submission.

I am grateful to my senior colleagues in the Electronics division Mr. A. V. Ananth, Mr. V. Chinnappan, Mr. G. Srinivasulu for useful discussions at times. I am thankful to Mr. J. S. Nathan for the help in providing computer facilities. I am thankful to Mr. A. S. Babu, Mr. M. R. Somasekhar, Mr. C. V. Sri Harsha, Mr. D. Babu for providing the electronic assistance at all times during the development of CCD camera system. I also thank Mr. K. C. Thulasidharan, Mr. M. S. Sundara Rajan, Mrs. Fassehana, Mrs. Padma for their support. I express my thanks to Mr. N. Jayavel and Mr. P. Janakiram for providing the mechanical support.

I have had full support from the electronics personnel at our field station, Vainu Bappu Observatory, Kavalur, from the beginning. In particular, I would like to thank Mr. K. Ravi, Mr. S. Venkateswara Rao, Mr. P. Anbazhagan, and Mr. A. Ramachandran for their wholehearted support. I am also thankful to Mr. S. Ramamoorthy, Mr. N. Sivaraj, Mr. J. Manoharan, and the observational staff at Kavalur for their cooperation during trial observations at the 1-m telescope. My sincere thanks to Mr. F. Gabriel, Mr. Mani, K. S. Subramaniam and other mechanical & electrical staff at Kavalur.

I would like to thank Dr. Vijay Mohan of State Observatory, Nanital for coordinating during cluster observations and immense help during data reductions. I am also thankful to the observational and technical staff at the State Observatory, Nainital. I also thank Mrs. Annapurni Subramaniam for providing information on cluster studies.

I would like to thank Mr. Sagay Nathan for the support during fabrication & assembling of the cryostat and integration of CCDs. I am also thankful to the Mr. Thimmayya and Mr. J. P.A Samson for extending their support when needed. I am grateful to Mr. Kamath and Mr. Mahesh for useful discussions and material procurement. I would like to thank Mr. V. K. Subramanian for the CAD support. I would also like thank the Photonics division for providing necessary help when approached.

I would like to thank the Library staff for their assistance and binding section for their help at various times. I sincerely express my thanks to the stores and administrative staff for providing instant help when needed.

Finally, I am thankful to my family members for silently bearing my responsibilities at home. Thanks to my wife, Chandrika, and children Navya and Bhuvan Sai. My mother, Jayamma, is always instrumental in my career and I remain indebted to her.

Abstract

Mosaic CCDs are particularly useful in imaging large size celestial objects like open clusters, globular clusters, galaxies etc. In such studies, a wide field coverage in a single observation run reduces the observation time at telescopes which otherwise might have required as many observational runs as the number of individual CCDs in the mosaic configuration.

Imaging with mosaic CCDs has received considerable attention in the past few years following the availability of buttable CCDs and fast Digital Signal Processors (DSPs). The advent of computer technology in hardware and software has given a scope for the development of powerful general-purpose CCD camera controllers. The DSPs offer flexibility, configurability and high-speed data acquisition needed for building such camera controllers. While the clock generation and data acquisition functions are met by a front end DSP, large data storage, powerful graphics display and processing functions are best handled by a host like Pentium PC. Such general purpose camera controllers which can operate mosaic CCDs are not available commercially. As a next step to the mosaic controllers specifically developed for a specific research needs, it is considered appropriate to develop a general purpose controller which can easily be programmed to suit any CCD or combination of such CCDs. Usually any hardware change in the camera such as that of a CCD chip to suit specific imaging requirement results in a corresponding change in the controller which imposes long lead time in the development phase. A software approach in such a situation ensures a reduction in the development and turn-around time. The host interface itself can easily accommodate the changes through its application software.

Keeping these factors in view, a general-purpose flexible CCD camera controller which can address any CCD or mosaic CCDs has been developed at the Indian Institute of Astrophysics (IIA). The primary design goals that need to be met can be summarized as follows.

1. A flexible, modular and re-configurable controller which meets various requirements in a simple way.

2. A powerful front-end controller which controls the camera controller functions and a host interface which provides a state of the art graphical user Interface, data acquisition, display and data reduction functions.
3. A loss-less on-line data compression resulting in reduction in data storage and bandwidth required for transmission.
4. A controller configurable for remote operation.
5. Provide an integrated environment with distributed computers implementing various other functions such as telescope control, dome control, back-end instrument control etc.

During this thesis work, a general purpose CCD camera controller based on a DSP has been successfully built and configured for a mosaic of 2x2 3-edge buttable Thomson-CSF CCDs (THX7897M). The controller operates from an IBM environment with a custom-built host interface add-on card. The controller was also successfully configured and tested with two other CCD: the ST002AB (2Kx4K) and the SI424 (2Kx2K). A modular CCD cryostats has been developed to accommodate the 2x2 THX7897M mosaic CCDs, the ST002AB and the SI424 CCDs. CCD data acquisition and display software has been developed under Windows9X/NT environment to support the above CCD camera systems. A detailed characterization of the mosaic CCDs has been carried out and few problems faced with THX7897M CCDs and their solutions are reported. The mosaic CCD camera system has been used to observe an open star cluster NGC 6631 with 1-m telescope, State Observatory, Nainital (UPSO) in two pass-bands V and I. The photometric results obtained from the mosaic CCD system were compared with the results obtained from the previous observations of the same cluster by the UPSO CCD camera system. The details of observations and data reductions are presented. The estimated cluster parameters for NGC 6631 are reported for the first time.

IIA has recently completed a challenging task of setting-up a remote operated 2m telescope at Indian Astronomical Observatory at Hanle, Ladakh in the Great Himalayan region. As the optical imager (ST002AB) is one of the important back-end instruments, the new controller should prove to be very useful in meeting the imaging requirements with this telescope.

Contents

Chapter 1

Introduction

1.1 A brief review of advancements in scientific CCD imagers

Charge Coupled Devices have opened up an exciting new window on the universe for the astronomers. CCDs were first introduced to the imaging world by Boyle and Smith in 1970 at the Bell Laboratories (Boyle & Smith 1970). The initial concept was to develop an electronic analogue to the magnetic bubble memories in which a bit represented a packet of charges (Chang 1975). The working principles are described on an introductory level in Amelio (1974), Kristian and Blouke (1982) and on a more advanced level in Bluke et al. (1981) and Wright (1982). The work of Wright is particularly rich in various technical aspects and describes different type of CCDs. A wealth of technical and engineering details can be found in the notes privately distributed by J. Janesick of JPL. In 1974 Jet Propulsion Laboratory took a major initiative in the award of a contract with Fairchild to produce the first 100*100 pixels CCD. The rapid demand in the television market gave an impetus to the growth of CCD imagers.

The early CCDs suffered several limitations such as small size, poor response to blue wavelengths and high readout noise. The limitation in size was due to the fact that a large size semiconductor wafer fabrication increased the gate shorts or open circuits. The yield became poor and thereby the cost went up. With the advancement in silicon processing the

defects were overcome. Leading semiconductor manufactures like Tektronix, Marconi (EEV), Ford, Kodak, Thomson etc now routinely produces the 2K*2K and 2K*4K CCDs. For wavelengths shorter than 4000 Angstroms, the photons are absorbed in the polysilicon gate electrode structure thereby reducing the quantum efficiency in the blue regions. This difficulty faced in the early CCDs has been overcome by using lumogen or metachrome coatings, which act as wavelength converters by placing the re-emitted photons from the ultraviolet to the visible wavelength regions (Blouke et al. 1980, Viehmann et al. 1981). The blue response of the devices also improved by thinning the CCDs and using back illumination, which avoided obstructions from the front gate structure (Lesser et al. 1986, 1989, and 1994). The read noise of the CCD is decided by the on-chip output amplifier structure. The challenge with the CCD manufacturers was to find an optimum amplifier geometry that yielded the lowest noise (Boulke, 1989). Today several manufacturers are fabricating CCD amplifiers that exhibit noise levels of 3 e- rms and lower by clocking the CCD in slow-scan mode. One can now do photometry with the CCD detectors down to 26^{th} magnitude and spectroscopy down to 23^{rd} magnitude. Such limits were simply unthinkable with the detectors of pervious generation.

2. Need for wide field imaging in astronomy

Wide field imaging has gained considerable attention in recent times in the study of open and globular clusters, galaxies and star forming regions. A study of star clusters provides valuable information on the process of star formation, stellar evolution and the properties of host galaxy. To understand the stellar evolution from the color magnitude diagrams (CMD) of the star clusters, rich open clusters containing more than 1000 star members need to be observed so that all the evolutionary stages in the CMD are populated with sufficient number of stars. These star clusters span large area in the sky, which demands large area focal plane optical imagers.

3. Mosaic CCDs

A cost-effective approach in realizing a large CCD is to mosaic the standard size CCDs that are produced with excellent yields at moderate cost. The mosaic CCDs readily form large area focal plane imagers, which reduce considerably the observing time required to cover the cluster when compared with a single CCD use. A variety of designs with 2 and 3-edge buttable large size CCDs are gaining popularity. Such buttable CCDs can be mounted carefully close to each other in various configurations to realize large size imagers (Reiss et al. 1989, Geary et al. 1991). A number CCD groups have developed large focal plane detectors deploying 2 and 3 edge buttable CCDs for use in their scientific programs (Luppino et al 1992, Stubbs et al 1993, Boroson et al 1994, Iwert et al 1993). A few mosaics using an array of packaged devices like TEK 2K, TEK 1K have also been reported (Sekiguchi et al 1992, Tyson et al 1992).

4. Scope of the IIA mosaic CCD camera system

A CCD camera system normally consists of a single CCD installed in a cooled detector head, a driver electronics unit and a PC host computer with a special purpose interface board. The mosaic CCDs pose new challenges in the cryostat fabrication, controller design and data acquisition and processing software. The mechanical mounting and the alignment of individual CCDs are rather critical. More the CCDs in the focal plane, more the thermal mass, calling for large volume cryostats. Mosaic CCDs also need a new controller with modular, flexible and programmable features so that the design efforts can be put to use in varying requirements. A mosaic of four 2K* 2K CCDs generate 32 megabyte of data per frame. This huge data needs to be displayed and stored in a combatable format for easy astronomical data reduction. In order to reduce the memory and disk space for the image data and bandwidth required in transmission for remote operation, a loss-less data compression is useful. The operation of a CCD camera in an integrated environment with the telescope and dome servers generates a need for a communication layer. Such a general-purpose camera controllers are not available commercially for the mosaic CCD operation.

With this background in mind, the development of a versatile CCD camera controller was taken up at the Indian Institute of Astrophysics.

5. Organization of this thesis

The work carried out in implementing a complete mosaic CCD camera system covering a modular cryostat, a flexible camera controller, a Pentium PC compatible host interface and a window based data acquisition and display software is reported in this thesis. It comprises of 7 chapters. The first chapter covers a brief overview of the progress in scientific CCDs and establishes the importance of wide field imaging in astronomy. The scope of the IIA mosaic CCD system is also addressed.

In Chapter 2, we present the design details of a modular CCD cryostat built for mounting and cooling the mosaic CCDs. An analysis of the heat losses and details of thermal insulation of the liquid nitrogen container are also included. Selection of materials and their processing and handling of out-gassing are described. The vacuum and liquid nitrogen holding performance attained by the cryostat is also presented.

In Chapter 3, we set the design goals to be met by a general purpose CCD controller. The hardware design details of such a controller are presented. The steps involved in configuring a camera controller are listed. The mosaic CCD controller built for operating a 2x2 mosaic of TI IX 7897 CCDs is described. A hardware based on-line data compression unit has been built and the details of its implementation and integration into the CCD controller are also presented.

In Chapter 4, we present the details of the data acquisition and display software developed for the CCD camera system. The advantage of object oriented programming over the conventional programming is listed. Design and implementation of the user interface is described. The flexibility of the software in configuring for the mosaic and other CCD cameras is illustrated. We also describe a messaging layer implemented using sockets with which the camera controller can support remote operation. Certain utility software functions such as photon transfer plot and filter-wheel selection also have also been added.

In Chapter 5, we describe the experimental setup used in characterizing the mosaic CCDs and the laboratory measurements which determine the noise, gain, linearity, quantum efficiency and defects / traps. The problem of crosstalk faced with the THX 7897 CCDs are listed and a solution is offered. The performance of the mosaic CCD camera system is evaluated by taking up observations of an open cluster NGC 6631.

Chapter 6 presents the observational details, data reduction methods and the CMDs obtained for the cluster NGC 6631. We estimated the cluster parameters and the field star contamination. The CMD of the cluster was used in determining the cluster distance and its color excess. The age of this cluster was determined with the help of the Bertille isochrones which points to a metal-rich model for the star cluster NGC 6631.

Chapter 7 summarizes what has been achieved during this thesis work. This chapter also describes the laboratory experiment conducted and its result. It then covers the study of the cluster NGC 6631 and the results obtained. A few suggestions on possible improvement to the present camera systems are also listed.

Chapter 2

Implementation aspects of a modular CCD cryostat

2.1 Introduction

Scientific CCDs need to be cooled to about -100°C in order to reduce the thermally generated electrons to negligible levels. The most common ways to cool the CCDs are either thermoelectric cooling or cryogenic cooling methods. Thermoelectric coolers (TEC) are solid state heat pumps that utilize the Peltier effect. Single stage TEC's are commercially available up to 1" x 1" size which can produce a differential temperature of about 70°C. Multi-stage TEC's can achieve differential temperature about 130° (Melcor thermal solutions) but limited only to a small area (5mm x 5mm). Thus, small CCDs can use multi-stage TEC to meet the desired operating temperature. For the larger format and mosaic CCDs, cryogenically cooled dewars are designed (Luppino et al. 1992) to operate the CCDs at well below -100°C. Another option is recently commercialized and is based on the closed cycle refrigerator (Cryotiger, APD Cryogenics Inc). These systems are slowly gaining acceptance in astronomical CCD imagers.

We have developed a modular cryostat (Naidu, Srinivasan & Natahn 2001), which can house CCDs in various configurations. The CCD camera head can be configured easily for mounting CCDs like 2Kx4K SITe CCD, 2Kx2K SITe CCD and a 2x2 mosaic of TH7897 CCDs. For use in our study, a dewar has been fabricated at the IIA and integrated with a 2x2

mosaic of THX7897 CCDs in the camera head. The following sections present the details of the cryostat cover the mosaic mount and reports the performance obtained.

2.2 The CCD cryostat built at IIA

An assembly sketch of the dewar is shown in Figure 2.1. The dewar comprises of two parts: one is the LN2 chamber housing and other is CCD Camera head. The chamber housing encloses a 2.4-liter capacity liquid nitrogen (LN2) tank, liquid fill & vent structure, vacuum port and activated charcoal plate attached to the liquid container. The LN2 tank is a thin-walled stainless steel, while the outer body is made out of an aluminum block. The thin-walls of the LN2 container reduces the cool-down time and the quantity of LN2 required for cooling the container itself. The SS exhibit high strength with excellent stability and toughness at low temperatures. A thin stainless tube of 200μm wall-thickness is welded to the back plate of LN2 chamber and other end of the tube is welded to a flexible SS bellow. The other end of the bellow is welded to a holder that is sealed with an O-ring against the inner surface of the rear flange. The LN2 container is firmly fixed to the outer body through a three-point support at 120° spacing.

The CCD camera head contains a mount base for a 2x2 mosaic of 3-side buttable Thomson CSF CCDs, an optical window and two hermetically sealed connectors for electrical signal feed through. The cold connection to the CCD mount from the LN2 chamber is established through a pair of copper straps held by a compressible spring. The CCD mount also incorporates a resistor heater and a temperature sensor. The camera head and the liquid chamber housing are vacuum-sealed by an O-ring and can be easily separated without any internal disconnection to the cold connection supporting easy maintenance.

2.3 Heat transfer & thermal insulation

There are three modes by which the heat enters the liquid vessel viz. i) heat transfer by gaseous conduction, ii) heat transfer by supports between the liquid vessel and the outer body and iii) heat transfer by radiation between the two surfaces. The most effective insulation between two surfaces at different temperatures is achieved when the space

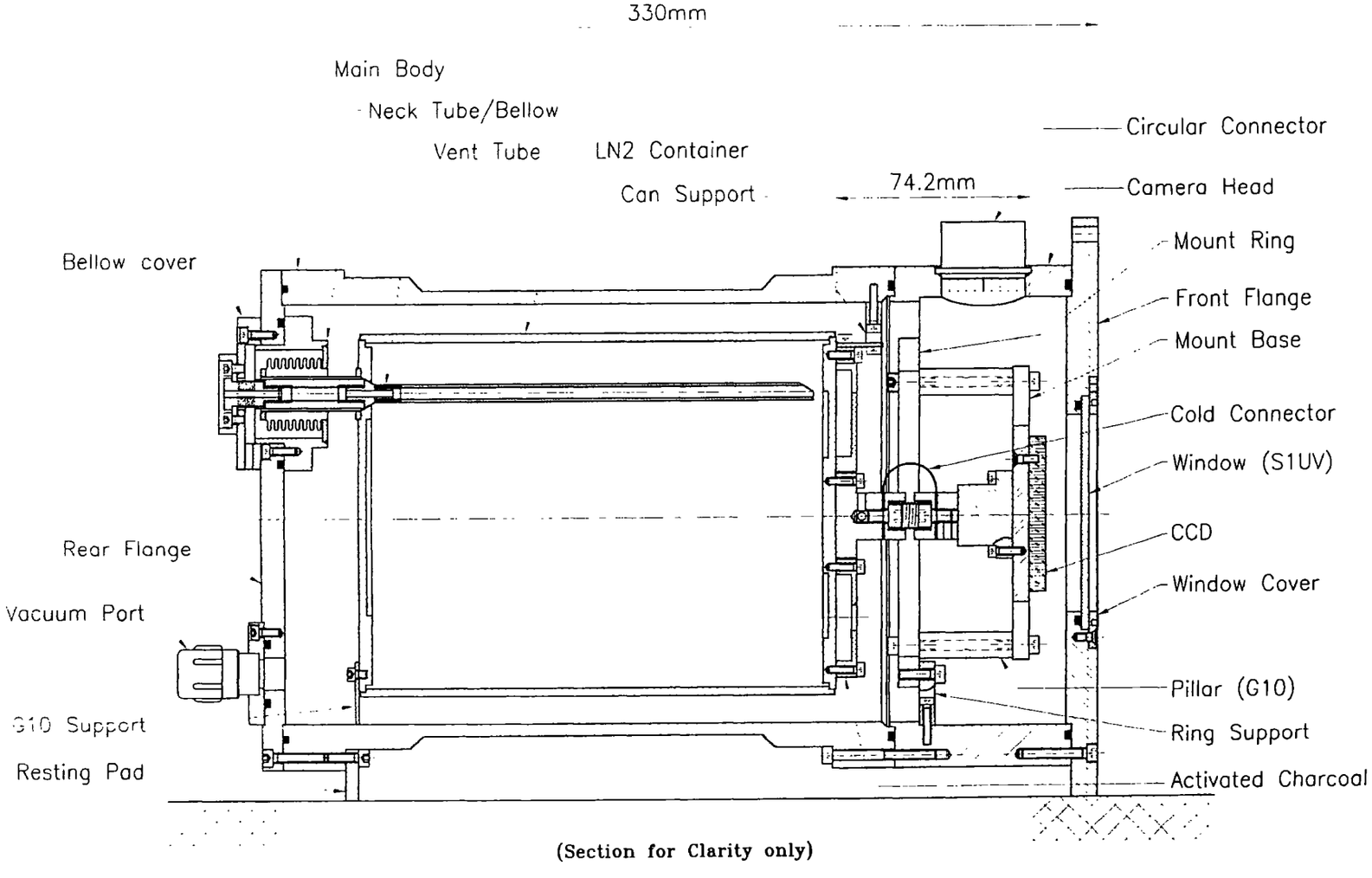


Figure 2.1: Modular CCD Cryostat

between them is evacuated. It is well known that the vacuum eliminates the gaseous conduction & convection and thus reduces the heat transfer. In addition to this vacuum insulation, if the heat transfer by radiation and conduction by support points are kept minimum, a good dewar can be realized. The inner surface of the outer body is buffed and cleaned to achieve the intrinsic reflectivity, while the outer surface of the liquid vessel is gold plated to reduce the radiation loses. The liquid vessel is held on the front side by three glass fiber spacers at 120° apart. Additional glass fiber bumpers are used on the back plate of the vessel at 120° spacing to avoid sagging against the outer body for side orientations. The main conduction losses occur through the liquid fill / vent structure. A thin neck-tube as shown in Figure 2.2 is used to reduce these conduction losses. The flexible bellow in the neck-tube assembly allows freedom for the thermal expansion / contraction during thermal cycling and also absorbs vibrations and shocks during the handling and transportation

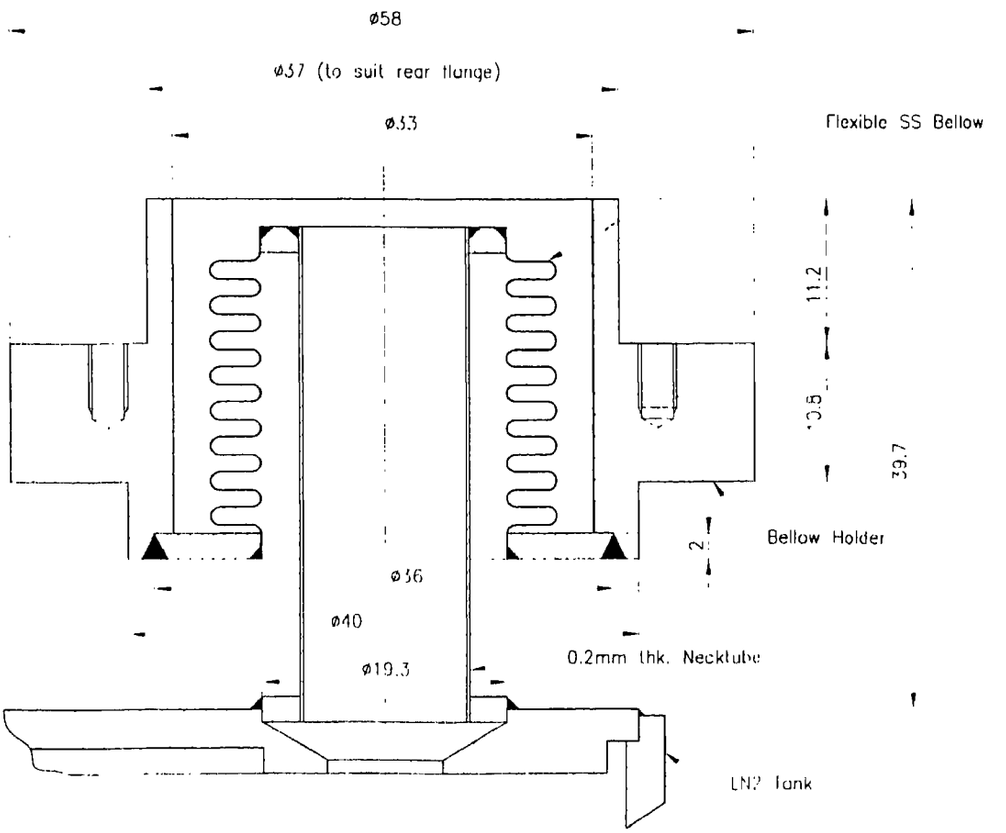


Figure 2.2: Bellow and thin neck-tube assembly

2.4 Handling of out-gassing

2.4.1 During fabrication

The material surfaces facing vacuum slowly release gases when the dewar is pumped and thus slow down the evacuation process. The degassing takes vary long time at room temperature. These gases can be easily removed by heating the enclosure while evacuating the dewar. It is also recommended to give heat treatment in vacuum oven for all the components to be used inside the vacuum, before assembling the dewar. Care should be taken right from the selection of materials (sources of contamination) to be used in the vacuum. PVC materials such as wires, heat-shrinking sleeves (solder joints) are to be avoided as they out-gas heavily. Fiberglass seems to produce no significant contamination in vacuum. Materials such as Teflon and epoxy resins are recommended.

2.4.2 During cold operation

The dewar needs to be evacuated until the cryostat reaches an adequate internal pressure (of the order of 10^{-6} mbar) to reduce the convection & conduction loses due to free gas molecules. Once the cryostat is cooled down, the free molecules can stick to and be trapped by the cold surface, which reduces the internal pressure. This process, called cryo-pumping, begins when the LN2 tank reaches near liquid nitrogen temperature. The dewar also incorporates activated charcoal to absorb the residual gas molecules into their surface pores and trap them until warm-up again. The charcoal is pasted using a low temperature adhesive to an aluminum plate and attached to the LN2 chamber so as to reach the low temperature of the liquid vessel. At room temperature, this adsorbent out-gases to some extent. As soon as the liquid is filled, the adsorbent becomes active and takes up the residual gases improving the vacuum inside the dewar. Molecular sieve can also absorb water vapor within the camera head. This prevents formation of frost on the CCD sensor when it is cooled below 0°C. Frost formation on the CCD lowers the image quality and also affects the multi-layer coatings on the CCD over time. Molecular sieve requires special handling, such as keeping the sieve component in a hermetically sealed, low humidity environment prior to installation. One

drawback with the molecular sieve is that its regeneration requires heating to about 200°C in vacuum for at about 20 hours. On the other hand, the charcoal getter can be re-activated just by pumping the dewar at room temperature. If the dewar is allowed to come to room temperature for quite some time, it is recommended to evacuate the dewar before filling the liquid.

2.5 Selection of materials, processing and assembling

One crucial part in the dewar is the thin neck tube with a bellow assembly. The bellow has wall thickness of 10 mils (0.25 mm). The bellow is welded to the neck-tube by laser welding. This assembly is fabricated and leak tested at Miniflex Corporation, USA. We used a thermally conductive epoxy, TEC-001 compound, which is Silver filled epoxy from M/s Melcor Thermal Solutions, USA to attach the activated charcoal pallets to an aluminum plate, which is mounted on the liquid container. This epoxy has low out gassing properties and requires a curing time of about 24 hours at room temperature. The optical window (S1UV fused silica with anti-reflection coatings on both sides), activated charcoal pellets, high vacuum grease and the vented screws are procured from GL Scientific, USA. The vacuum seal-off valve is procured from M/S Cryolab, Cireleseal contols, Inc. USA, and has 6mm port size. The hermetic connectors are supplied by M/S OEN, Kerala, India.

The liquid nitrogen container is made out of a SS seamless tube and two SS plates. The parts were finely machined and buffed and cleaned before welding. The back plate of the container is first welded to the Neck-tube collar of bellow assembly. Then the two SS plates were welded to two ends of the cylinder. The container is gold plated. All the other aluminum dewar parts were also buffed to get intrinsic reflectivity. All the parts were cleaned first by acetone or alcohol. The components were baked in a oven at about 60°C. Subsequently the parts were handled with clean room gloves and the cryostat is integrated in a clean environment (laminar flow) of class 100. After assembling, the entire dewar was baked to about +60°C while pumping to improve the vacuum.

2.6 Analysis of heat load

The Cryostat is designed to hold liquid nitrogen for more than 24 hours in normal operation. The liquid hold-time coefficient of the dewar is calculated as follows.

Liquid hold-time coefficient = Liquid volume * Heat of vaporization of LN2

= 2400ml * 160J/ml

= 2400 160 * 2.77 *10^{-4} Whr.

= 103.68 Whr.

In order to obtain more than 24 hours of holding time, the total heat load on the dewar should be less than 4 W.

The actual heat load on the container can be calculated by considering the three modes of heat transfer (Thomas M. Flynn 1997). At pressures bellow 1 mbar range, the rate of conduction by gas molecules is nearly proportional to the gas pressure. Since the dewar is evacuated to well bellow 10^{-3} mbar, and the charcoal getter keeps the dewar evacuated at around 10^{-3} mbar as long as the liquid is present, the conductive heat gain by the residual gas molecules is negligible. The conduction and radiation losses are calculated as follows.

2.6.1 Conduction through support structures

The heat gain by the LN2 chamber supports, through the neck-tube/bellow assembly, CCD mount supports and due to wires are calculated using

$$Q_c = (kA/L)*(\Delta T)$$

Where, A is the cross sectional area, L is the length and k is the thermal conductivity of the support member. ΔT is the difference in the temperature between the two ends. Table 2.1 lists the various conduction losses in the system. The total conduction losses add to 2.5W.

Table 2.1: Summary of main conduction loses

Structure	Material	(k) (mW/cm.K)	A/L (cm^2/cm)	ΔT	Qc (mW)	Qua-ntity	Total (mW)
LN2 main supports	Glass Fiber	10	0.09	220	198	3	594
LN2 side supports	Glass Fiber	10	0.03	220	66	3	198
Neck-tube	SS304	110	0.03267	220	790	1	790
CCD mount	G-10	4	0.4167	120	200	4	800
Wires	Const-antan	200	0.0000049	120	1.18	25	30

2.6.2 Radiation losses

The rate at which a surface emits thermal radiation is given by the Stefan-Boltzmann equation

$$Qr = \sigma e A T^4$$

Where e is the emissivity at temperature T, A is area and σ is constant having 5.67 x 10^{-12} $W/(cm^2.K^4)$. So, the net exchange of radiant energy between two surfaces at two different temperatures T1 and T2 is given by

$$Qr = \sigma e A(T2^4 - T1^4)$$

where A is inner surface area. Assuming the parallel plate geometry between the LN2 container and the outer body, the emissivity can be taken of the form

$$e1e2/(e2+e1(1-e2))$$

where, e1 and e2 are the emissivities of the cold and warm surfaces at T1 and T2 temperatures.

Since the inner surface of the outer body is made reflective and the LN2 vessel is gold platted, and by using low emissive materials wherever possible the heat transfer by radiation

is kept less than 400mW. Table 2.2 lists the radiation losses due to the cylindrical and parallel surfaces in the dewar.

Table 2.2: Summary of radiation loses

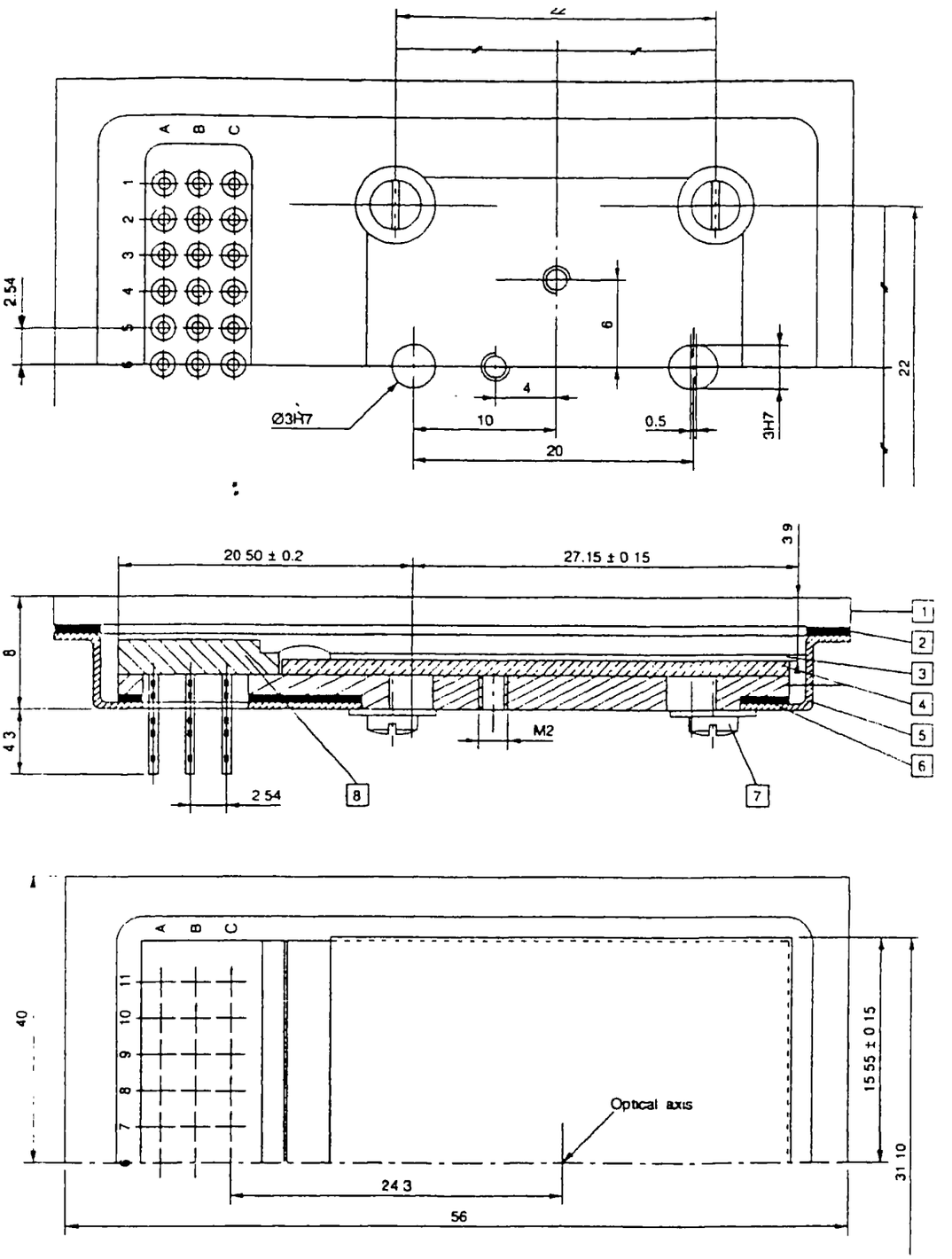
Surface	Inner Surface (Gold plate on SS) (77K)	Outer Surface (Aluminum) (300K)	Area (inner surface) (cm^2)	Qr (mW)
Cylindrical	e1 = 0.01	e2 = 0.03	792	274
Parallel (top)	e1 = 0.01	e2 = 0.03	154	54
Parallel (bot)	e1 = 0.01	e2 = 0.03	154	54

The CCD self-dissipation (assumed to be less than 100mW) in its normal mode of operation is also added to the total heat load. Hence the total heat gain (Qc + Qr) by the LN2 chamber is less than 3W.

2.7 The mosaic CCD mount

A clean air laminar flow facility for handling the CCDs has been setup. The mosaic CCDs were integrated under a clean environment of class 100 laminar flow. Pre-filters are made-up of polyester fiber medium with both the sides reinforced with HDPE mesh and protected by perforated sheet. Collection efficiency is 90% for particles > 10 microns. The post filters are made from ultra-clean glass fiber paper medium separated by aluminum corrugated foils. Collection efficiency is 99.97% for particles > 3 microns. The clean environment encloses an anti static workstation, required for the safe handling of CCDs. The floors have a static dissipative mat and the tabletop where CCDs are handled also has static dissipative laminate. An ionizing grid is also used to reduce the background ESD to safety levels.

Figure 2.3 shows the mechanical details of the TH7897 CCD. The individual CCDs are mounted onto a 6mm thick molybdenum base plate, which is ground flat. This mount plate is thermally isolated from the outer body and supported by four G-10 pillars. Mounting



1 Window
2 Silicone seal
3 CCD
4 Cu W base + diver
5 Protective cover
6 Silicone seal
7 Screw
8 Ceramic

Figure 2.3: Mechanical details of THX7897

holes were drilled on the base plate at the selected positions in order to accommodate the four CCDs. Locating pins have been provided for each CCD to facilitate easy installation of the device onto the mosaic plane. The CCDs are handled with a rod, which screws on to the back of the CCD. The handling rod along with the two locating pins for each CCD (one fixed on to the back of the CCD and the other on the mount base) prevents the CCDs from touching each other while installing on the plane. Each CCD is fastened to the base plate through a set of 4 screws. The inter-gaps between the CCDs are held within 1mm. The backside of the mount plate accommodates two resistor heaters and a temperature transducer. The CCD mount is cooled down to -90°C. Figure 2.4 presents the details of the mosaic CCD camera mount. Constantan wires (0.01") with a PTFE insulation are used in bringing out the CCD connections to the connectors, except for the CCD output and ground signals, which use thin copper wires.

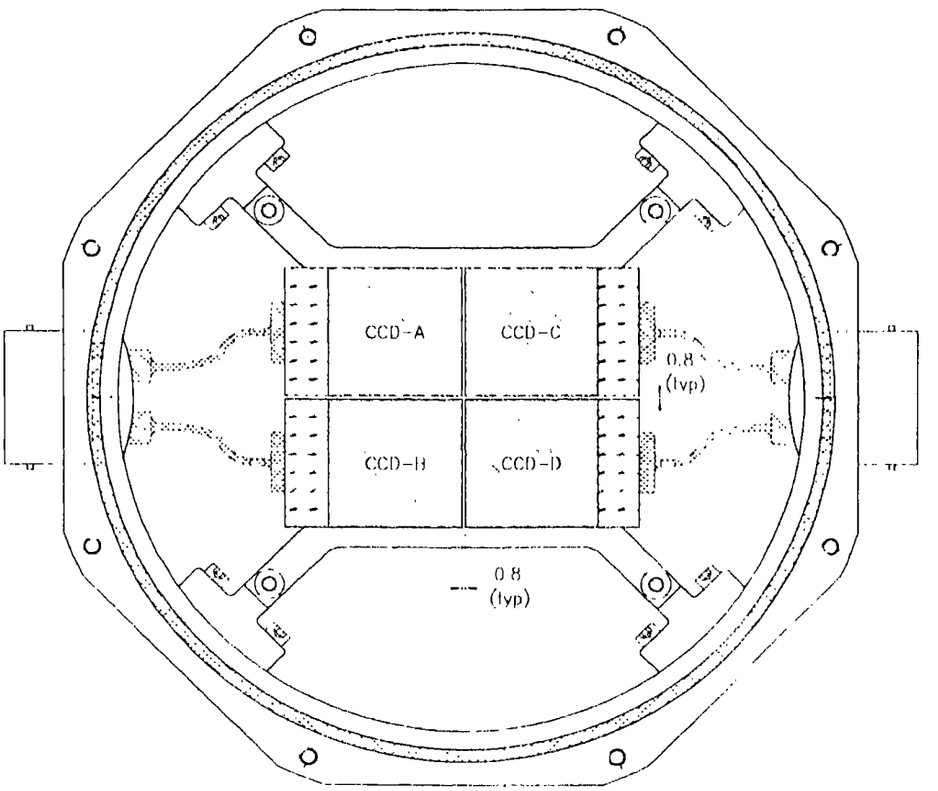


Figure 2.4: 2x2 mosaic of YHX7897M CCDs.

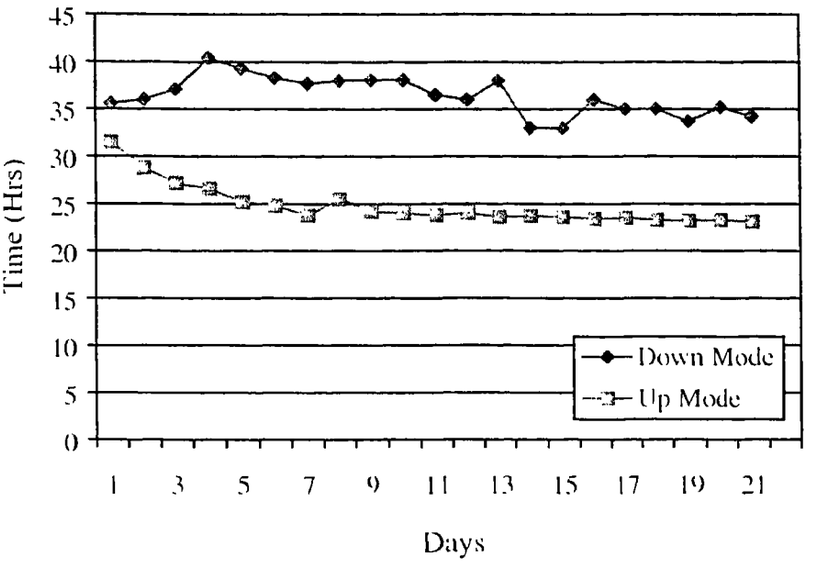


Figure 2.5: Liquid hold times of the cryostat

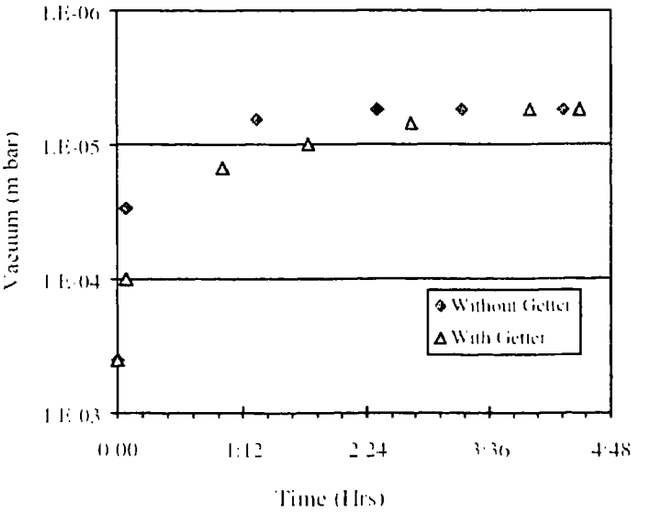


Figure 2.6: Vacuum build up of the cryostat.

2.8 Performance

The initial cooling of the CCD mount takes about an hour to reach its operating temperature. Figure 2.5 illustrates the liquid hold-times obtained in normal and inverted modes of operation. The liquid nitrogen holds for over 32 and 24 hours in the normal and inverted modes of operation. In the inverted modes of operation, the hold time comes down due to the conduction losses through the vent tube that needs to be installed to avoid spilling of the liquid. The liquid hold time is obtained by measuring the rate of evaporation of the liquid. Figure 2.6 shows the build-up of vacuum of the dewar with time when used with turbo molecular pump (TMP- V250). The dewar holds satisfactory vacuum level for an average two months. Thus the dewar met the two important requirements of holding vacuum for a reasonable period and a cryogen holding time of at least 24 hours in any mode of operation.

Chapter 3

Hardware details of the IIA CCD controller

3.1 Introduction

A general purpose CCD controller calls for a new architecture with modular, flexible and programmable features so that varying requirements can be met. It is best to configure a hardware design which can support a variety of CCDs. Early CCDs incorporated a single readout due to their limited size. As the CCDs grew in size, multiple readout devices became necessary in order to reduce the frame readout time. As such CCD controllers are not commercially available for the mosaic CCD operation. In this context, a versatile CCD controller based on a Digital Signal Processor (DSP) has been developed for scientific CCDs. DSPs offer speed, flexibility in configuring the waveform sequencer for the CCD controllers and in acquiring & transferring data to the host computer. The following sections present the controller design details and its implementation for the mosaic CCDs.

3.2 The controller design goals

As the early controllers for the CCD camera systems addressed a single CCD with a single readout, the timing generation could be met with simple schemes ranging from hard-wired logic circuits to programmable EPROMs (Naidu et al., 1998). These systems became complex as modification to the clocking sequence arises during the course of development. The new generation controller should be a general purpose that can be used for any CCD or mosaic CCDs. A few researchers have reported controllers developed for

mosaic CCDs in the recent past (Reiss 1994, Leach & Beale 1990, Leach & Denune 1994, Smith 1996 and WonYong 1996) based on digital signal processors, transputers and programmable logic devices (PLD).

Before presenting the details of a new controller design, it may be appropriate to give an outline of the design requirements. The design requirements can be summarized as below 1) The controller should be a general purpose one so that it can operate different CCDs from various manufacturers. 2) The bias and clock voltages should be programmable so as to allow easy tuning of the parameters. 3) The controller should be flexible to accommodate various modes of operation like window readout and binning of the pixels. 4) The controller should be modular in design so that features like signal processing or timing generation can be easily configured to suit specific requirements. 5) The controller should support hardware compression techniques.

With the requirements as laid above, a new versatile CCD controller has been designed that meets all the design requirements based on a PC host interface and a Motorola DSP (M56002) front-end controller (Naidu and Srinivasan, 2001). We describe the hardware details of the controller and in particular the implementation of a 4K x 4K mosaic using four 2K x 2K Thomson TH7897 CCDs used in our cluster study. In this controller each CCD in the mosaic is driven separately and the individual CCD clocks & bias voltages can be tuned to optimize the performance. The basic units of the controller are described in the following sections.

3.3 Hardware details

A block diagram of our camera system is shown in Figure 3.1. The camera design centers around an IBM PC host computer and a DSP based CCD controller. The PC platform was chosen due to its low cost, easy maintenance and powerful hardware and software supports. A custom built add-on card forms the host interface for the CCD controller. The host configures the CCD controller for specific CCDs and for different modes of operation. It receives the CCD image data displays and stores the data in FITS format for compatibility with other data reduction software like IRAF. The host also provides some analysis functions for quick a look at the acquired data. The CCD controller accepts commands from the host, generates various timing signals for serial & parallel clocks and controls various analog processing functions like double correlated

sampling (DCS). The controller digitizes the processed analog data and transfers the data into the host computer.

The controller architecture comprises of four major functional units in addition to a power supply module:

- DSP CPU board
- Bias & Clocks board
- Signal-processing board
- PC interface card

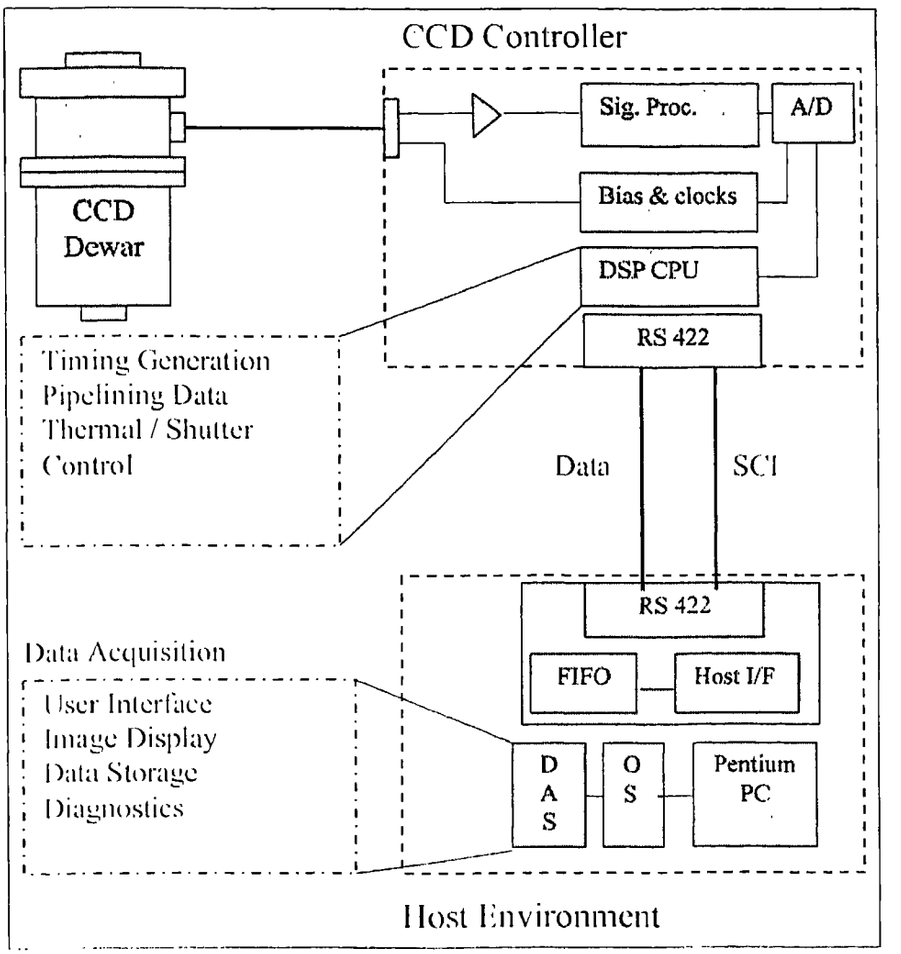


Figure 3.1: Block diagram of CCD camera system.

These boards are 6U in height (233 mm) and 160 mm in depth. The backplane uses two Euro connectors for each card (like VME standard) and can accommodate 9 PCBs. In a 4 CCD mosaic system, 4 bias & clocks boards, 4 signal-processing boards and one DSP board can be installed on the backplane. This configuration permits simultaneous

control of the CCDs and readout from their channels. In the case of a single CCD, a different back plane can be used which holds a DSP board, one bias & clock board and one signal processing board. The communication between the host computer and the camera controller for bootstrapping and commands is implemented through a serial communication link (Tx, Rx, Clock) while the CCD data acquired by the DSP controller is transferred to the host computer through an 8 bit parallel port.

3.3.1 DSP CPU board

This board is responsible for the timing sequence, programming the bias and clock voltages, and generation of hand-shaking signals with the host computer. The Motorola DSP M56002 forms the heart of this mosaic controller design. The DSP56002 is chosen for the following reasons. i) Highly reduced instruction set, ii) High speed (20MIPS) of operation, iii) Built-in memory (512 words of program memory, 2x512 words of data memory) iv) A small glue logic in implementing a waveform sequencer (Naidu and Srinivasan, 1996) and v) Bootstrapping capability from a serial communication link or from a host processor. The functional block diagram of the DSP CPU board is shown in Figure 3.2 and the schematic circuit is shown in Figure 3.3. The main functions of this board are i) to receive and execute the program code from the host, ii) to load all DAC's in the Bias and Clocks board, iii) to generate the timing signals for readout of all CCDs and iv) and to send the digitized data to the host with a strobe signal. The thermal and shutter controls are also included in this board.

3.3.1.1 I/O ports

The DSP has three ports. Port-A is the memory expansion port consisting of an external address bus (16-bits), data bus (24-bits) and control signals. The bus control signals allow read/write control, address space selection (program or data) and bus access control. Port-B is a dual purpose parallel I/O (15 bits) port that can be used as general-purpose pins independently configurable as inputs or outputs or an 8-bit bi-directional host interface. Port-C provides asynchronous serial communication interface (SCI) or serial synchronous interface (SSI) to other processors.

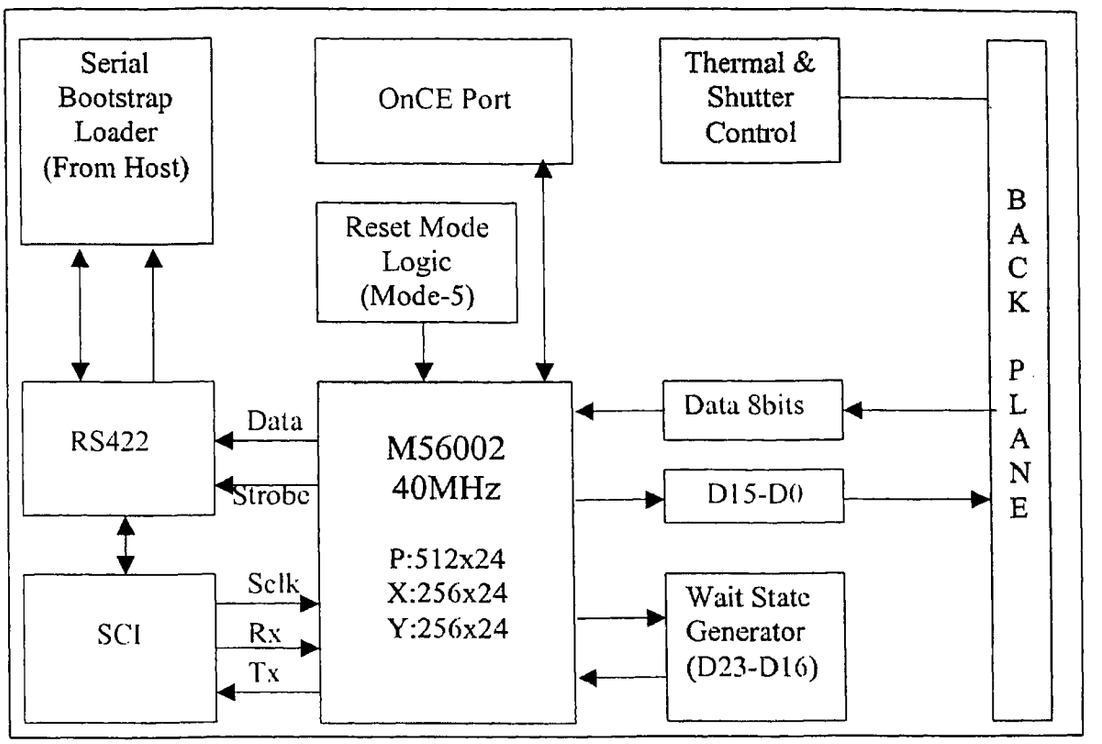


Figure 3.2: Functional block diagram of DSP CPU board

3.3.1.2 Port-A/B configuration

The entire CCD controller is operated from a 24-bit data bus (D23–D0) of Port-A with a few control bits from Port-B (PB0-PB4) of the DSP. The DSP writes a 24-bit data word on its Port-A containing a time field (most 8 bits) and 16 state bits as shown in Figure 3.4. The time field specifies how many clock cycles the sate bits shall hold these values. The DSP asserts DS' and WR' signals along with data on its port-A D23-D0. A non-zero data on D23-D16 sets an 8-bit comparator output (P=Q) to high level. A flip-flop (U39) sets its output high following the start of the write cycle, which triggers an up/down counter (U34) to count down. The counter starts counting down at the DSP clock rate from its initial value. The WT' (wait) input of the DSP is held low during the counting period and hence the DSP continues to insert wait states in its write cycle. When the counter reaches the terminal count, the counter output (TC') clears U39 which in turn allows the DSP to come out of inserting wait states and complete the write cycle. The DSP's write cycle can be stretched to a maximum of 6.4μs by programming the number

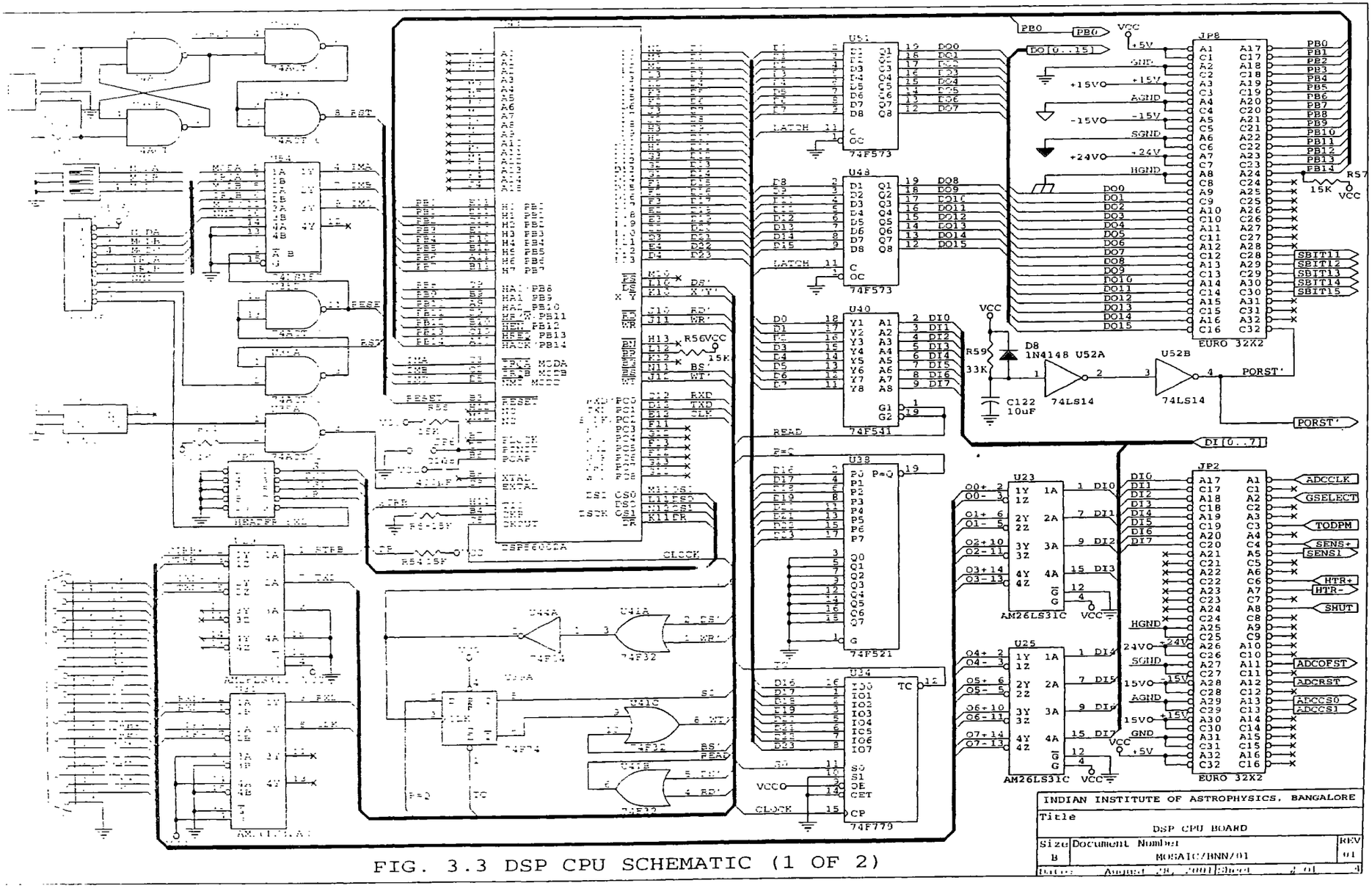


FIG. 3.3 DSP CPU SCHEMATIC (1 OF 2)

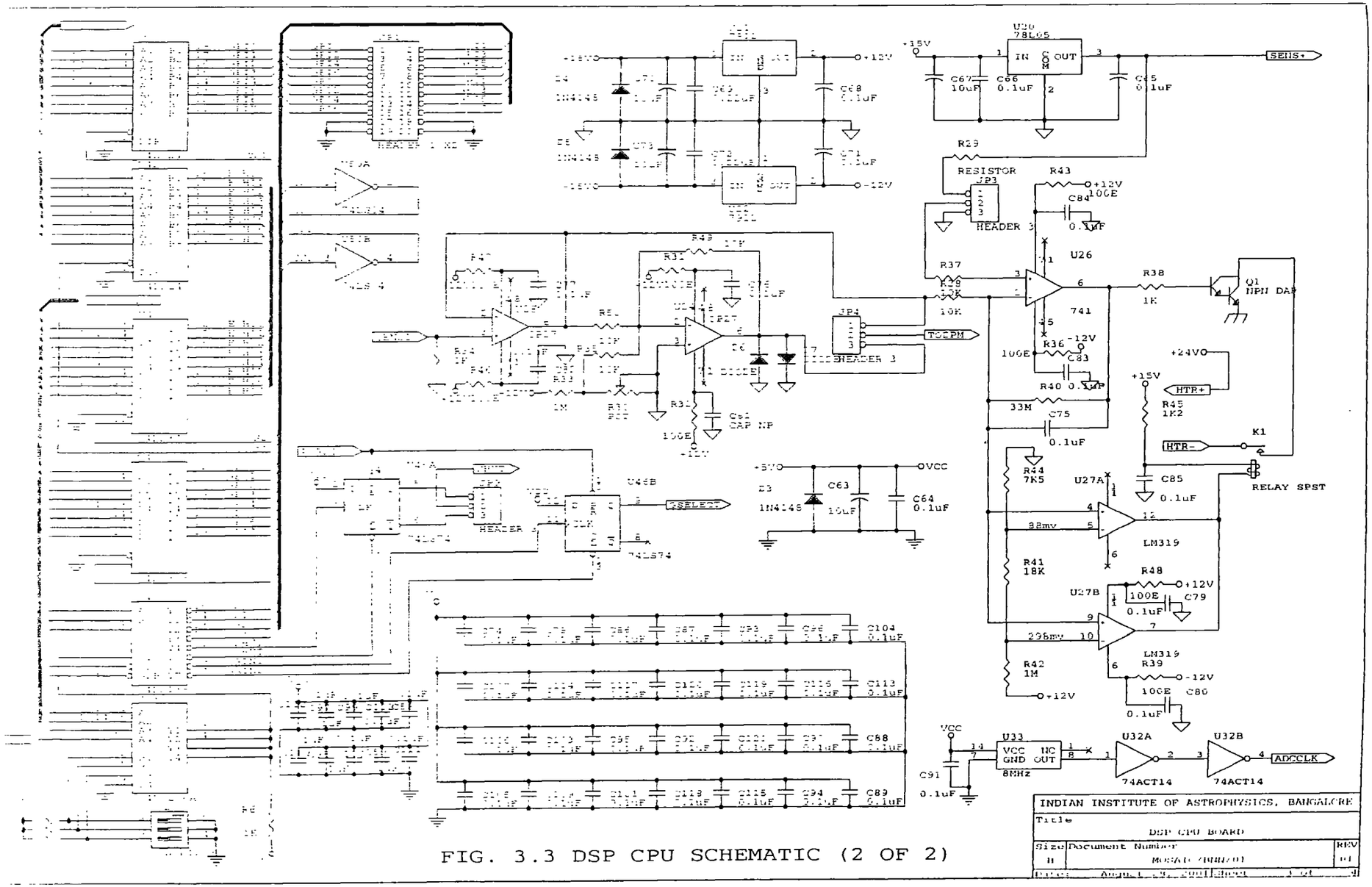


FIG. 3.3 DSP CPU SCHEMATIC (2 OF 2)

of DSP clock cycles. This feature implements the required delays between successive outputs without the need for any software delay loops. When PB0 is low, the bits D15-D13 select the bias & clocks board while the bits D12-D8 select which digital to analog converter (for setting up of bias and clock voltages) to load with the data present on the bits D7-D0. When PB0 is high, the bits D15-D0 represent the timing pattern required for the CCD readout and signal processing. PB1-PB4 select the individual CCD in the mosaic configuration. The DSP enables the digitized data byte at a time and also generates a strobe pulse on its Timer I/O (TIO) pin to transmit the data to the host computer.

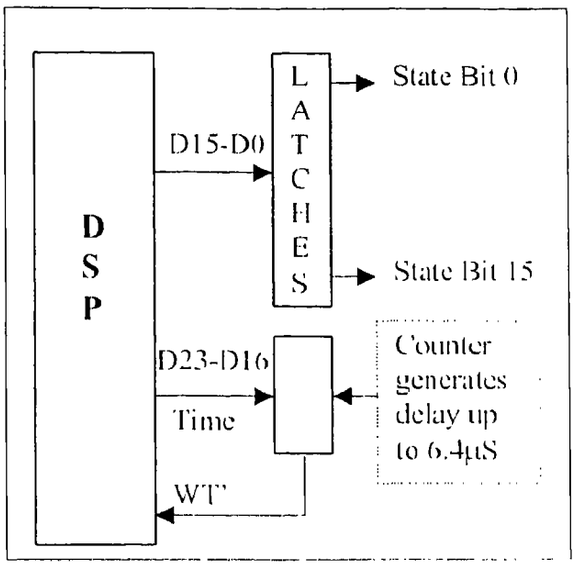


Figure 3.4: Timing Generation using state and time fields

3.3.1.3 Temperature controller

The CCD mount needs to be operated at a stabilized operating temperature in order to obtain a stable dark statistics. The temperature controller circuit for the mosaic CCD mount is incorporated in the DSP CPU board. The temperature sensor (AD590) provides a current output which produces 1mV/°K when terminated with a 1K Ω resistor. This signal is compared with the set temperature by a gain comparator (U26). The comparator controls a darlington transistor (Q1) to regulate the current in a heater resistor and thereby temperature in the camera mount. The range with in which the temperature control should operate can be set in a window comparator (U27). When the dewar is filled with LN2 the CCD mount is heated to the set temperature and stabilizes at the set

point with an accuracy of 1°. A shutter control mechanism generates the required exposure times. The shutter driver is configured external to the CCD controller.

3.3.2 Bias and clocks board

The Bias & Clocks board configures all the necessary bias and clock voltages required for a single CCD. Figure 3.5 shows the block diagram of the bias and clocks board while the schematic circuit is shown in Figure 3.6. This board decodes the 16 bit outputs (D15-D0) from the backplane. A board-select decoder formed by a 4-bit comparator (U26) and a dip switch (S1) decodes the output DO15-DO13 when PB0 is held low. This decoding allows up to 8 such boards to reside on the same data bus without conflicting with each other. The DO12-DO8 lines are decoded to provide the 24 chip select (CS0-CS23) signals. When the board gets selected, an octal buffer (U41) routes the data DO7-DO0 to the inputs of various digital to analog converters (DAC). Table 3.1 summarizes these decoding functions.

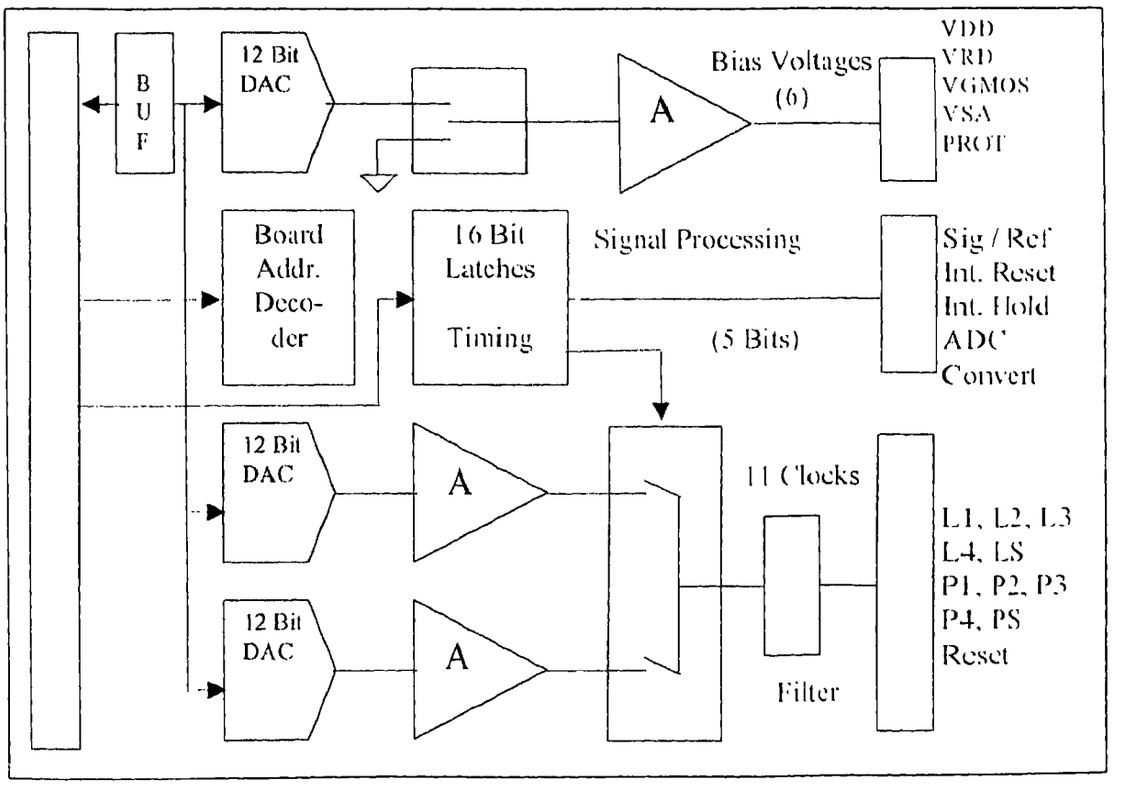


Figure 3.5: Block diagram of bias and clocks board

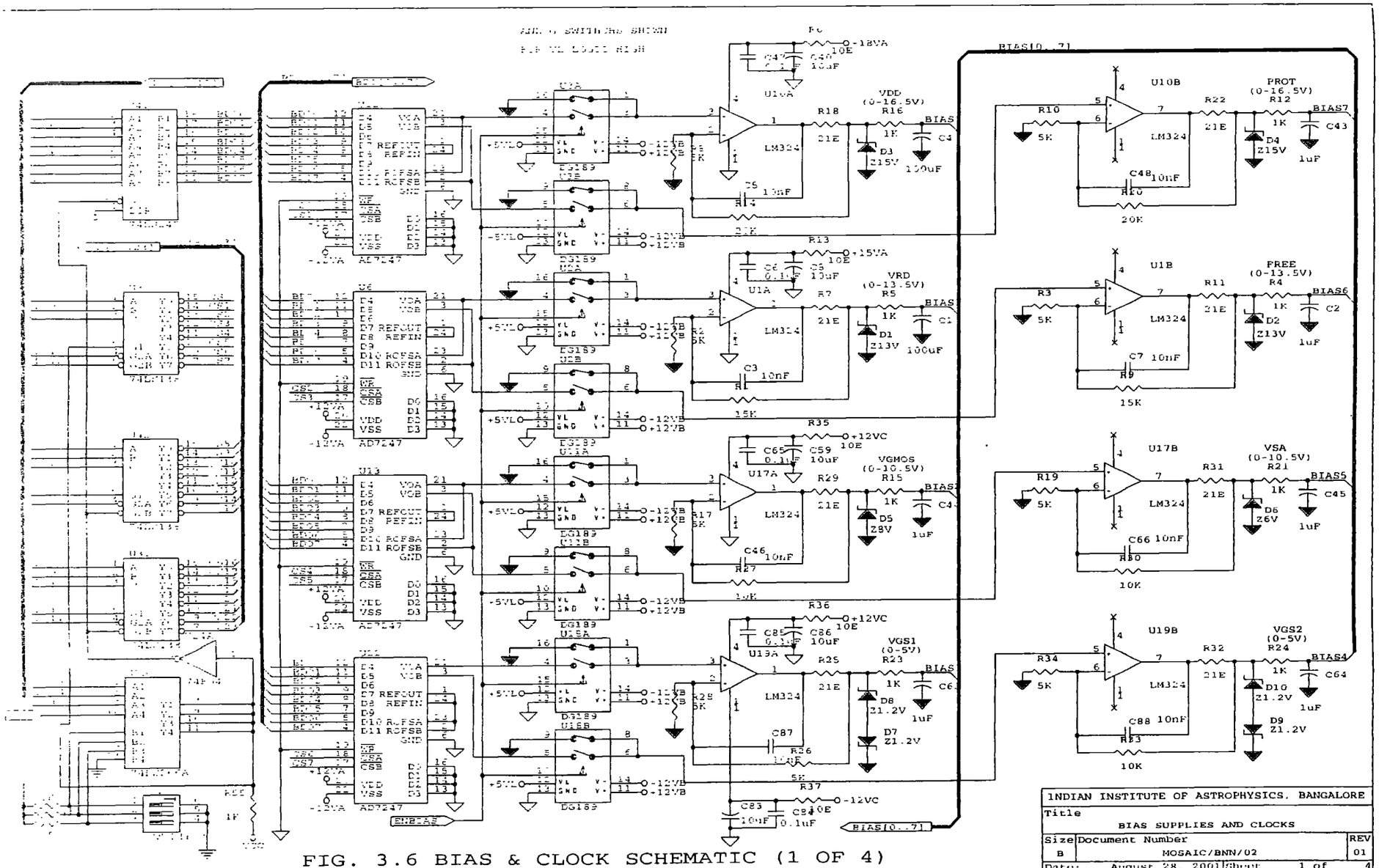


FIG. 3.6 BIAS & CLOCK SCHEMATIC (1 OF 4)

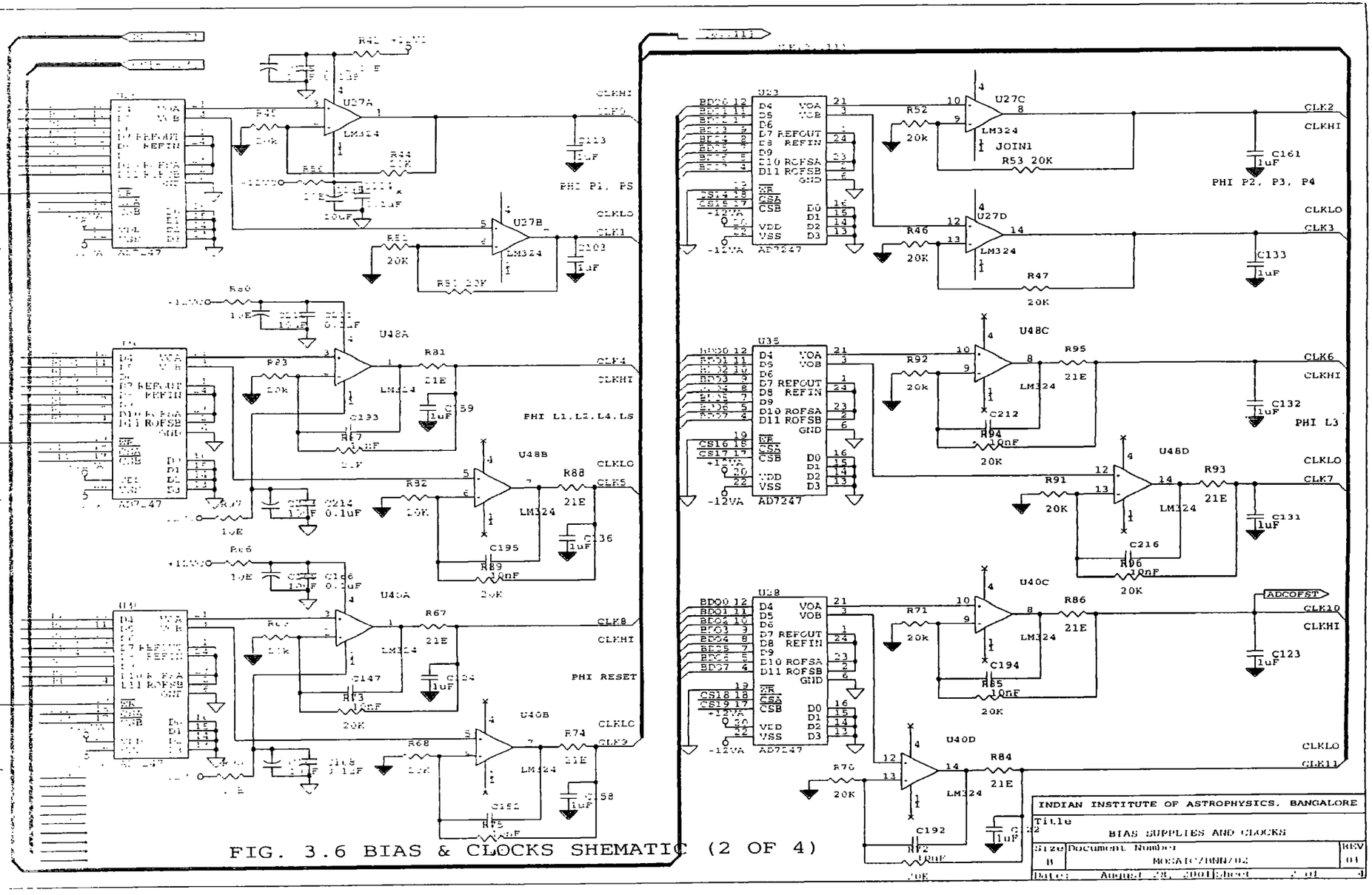


FIG. 3.6 BIAS & CLOCKS SHEMATIC (2 OF 4)

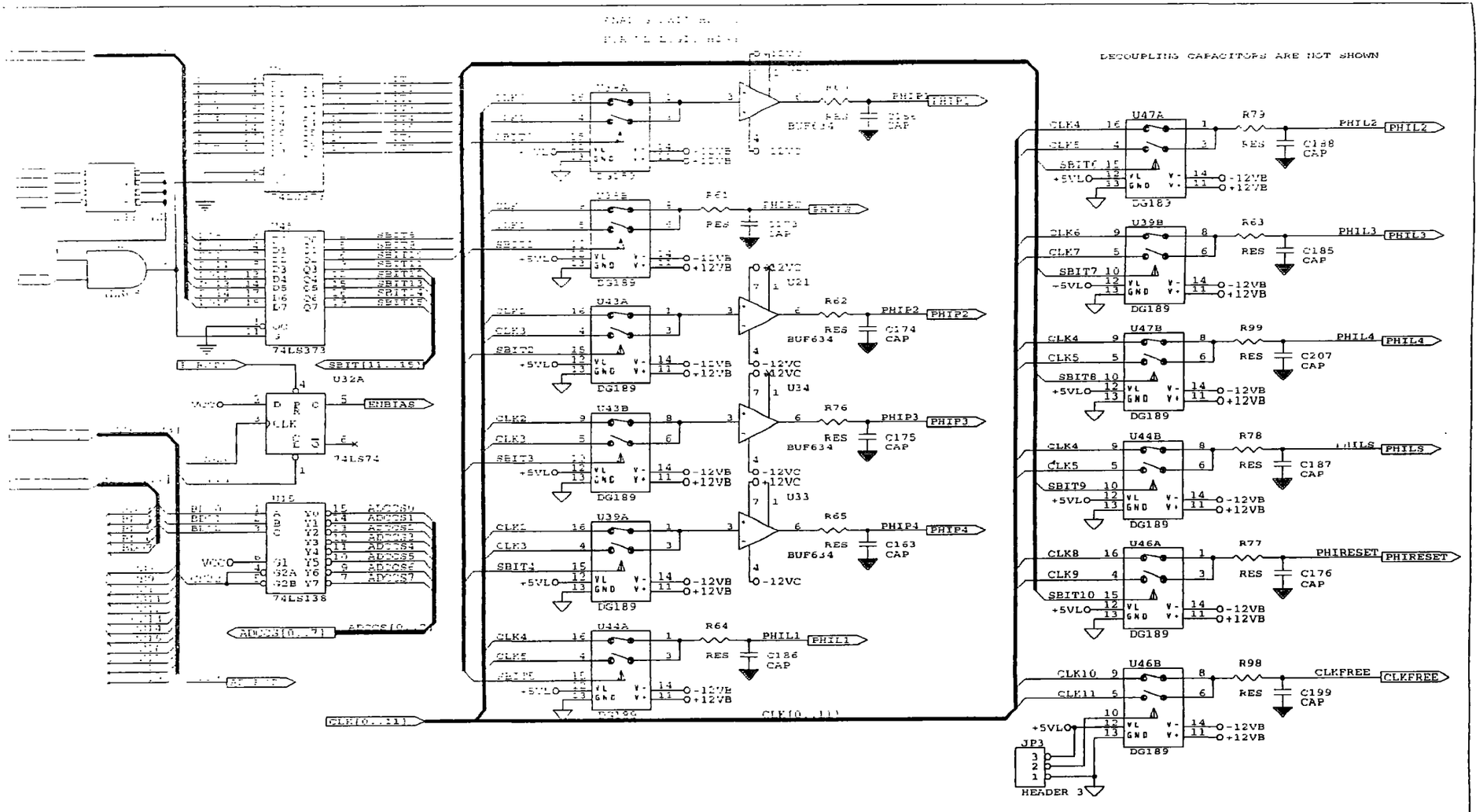


FIG. 3.6 BIAS & CLOCKS SCHEMATIC (3 OF 4)

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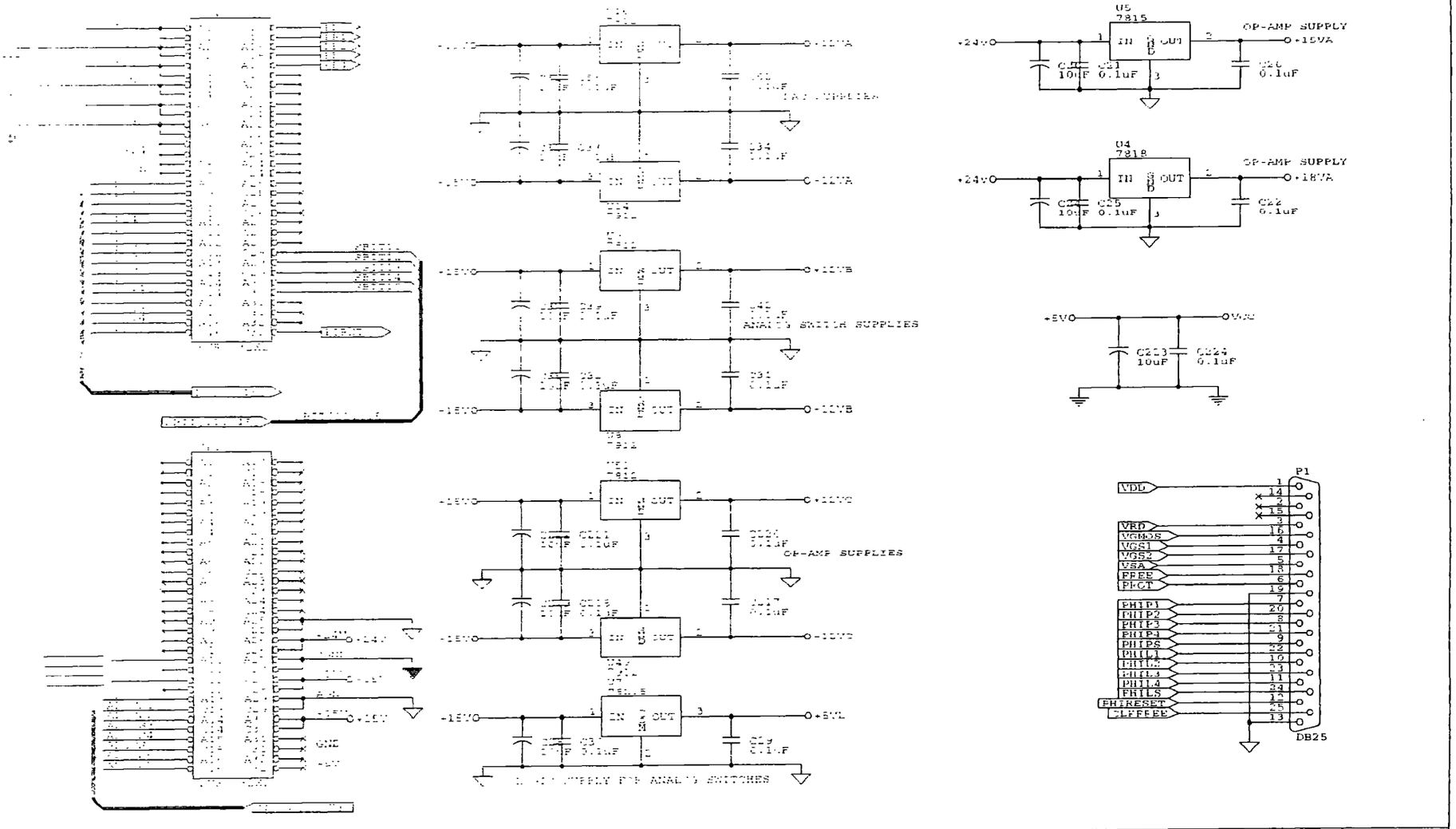

FIG. 3.6 BIAS & CLOCKS SCHEMATIC (4 OF 4)

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Table 3.1: Decoding

PB0	Data bits	Decoding function
Low	D15-D13	Selects one of the bias & clocks boards
	D12-D8	Provides 24 chip selects for bias & clock DACs
	D7-D0	Provides input data for the DACs
High	D15-D11	Control bits for the signal processing chain
	D10-D0	State bits for the serial / parallel clocks

3.3.2.1 Generation of bias voltages

The chip selects CS0 – CS7 select the bias DACs. Various bias voltages such as reset drain (VRD), output drain (VOD), on-chip current source FET gate voltage (VGMOS), output gate voltages (VGS1, VGS2) and source voltage (VSA) are generated using 12-bit DACs followed by suitable buffer amplifiers. Table 3.2 lists the bias details.

Table 3.2: Summary of bias voltage generation (for TH7897)

Chip selects	DAC	Buffer / Amplifiers	Gain	Range (V)	Bias selected
CS 0	U12A	U10A	5	0 to 16.5	Output drain
CS 1	U12B	U10B	5	0 to 16.5	Protection
CS 2	U6A	U1A	4	0 to 13.5	Reset drain
CS 3	U6B	U1B	4	0 to 13.5	Not used
CS 4	U13A	U17A	3	0 to 10.5	VGMOS
CS 5	U13B	U17B	3	0 to 10.5	VSA
CS 6	U22A	U19A	2	-5.0 to 5.0V	VGS1
CS 7	U22B	U19B	2	-5.0 to 5.0V	VGS2

JFET switches (SPDT) are used to cut-off the DAC outputs (and to ground the inputs of the bias drivers) until they are safely configured during power up. All the bias supplies can be enabled or disabled remotely from the host computer. The bias supplies incorporate limiting circuits using zener regulators to ensure safe operation of the CCDs.

3.3.2.2 Generation of clock voltages

The chip selects CS8-CS17 select clock voltage DAC's. Various clock voltage levels (high and low) of a clock are set by two 12-bit DAC's, followed by suitable buffer amplifiers. Table 3.3 summarizes the clock voltage generation.

Table 3.3: Summary of clock voltage generation (for THX7897)

Chip selects	DAC	Buffer/ Amplifier	Gain	Range (V)	Clock selected
CS 8	U25A	U27A	2	-10.5 to 10.5	P1, PS (high)
CS 9	U25B	U27B	2	-10.5 to 10.5	P1, PS (low)
CS 10	U36A	U48A	2	-10.5 to 10.5	L1,2,4, LS (high)
CS 11	U36B	U48B	2	-10.5 to 10.5	L1,2,4, LS (low)
CS 12	U30A	U40A	2	-10.5 to 10.5	Reset (high)
CS 13	U30B	U40B	2	-10.5 to 10.5	Reset (low)
CS 14	U23A	U27C	2	-10.5 to 10.5	P2, P3, P4 (high)
CS 15	U23B	U27D	2	-10.5 to 10.5	P2, P3, P4 (low)
CS 16	U35A	U48C	2	-10.5 to 10.5	L3 (high)
CS 17	U35B	U48D	2	-10.5 to 10.5	L3 (high)

When PB0 is held high, the octal latches (U50, U45) become transparent and DO15-DO0 serve as state bits for the clock generation (11 bits) and controls (5 bits) for signal processing chain. A high-speed analog switch selects these levels to the output depending on the state bits (SBIT0-SBIT10) derived from the timing sequence. Current buffers (BUF634, 1.5A) provided at the parallel clocks outputs drive the high gate capacitance at fast rates. A passive RC filter is incorporated at each clock output, which permits suitable edge shaping. The clock shaping is set for optimised charge transfer efficiency and minimises spurious charge generation. The Bias & Clocks board can produce 11 clock voltages that are fully programmable in the range −12V to +12V. Various clocks such as parallel clocks (P1, P2, P3, P4), parallel summing clock (PS), serial clocks (L1, L2, L3, L4), serial summing well (LS) and reset clock (R) are obtained from the timing state bits SBIT10-SBIT0.

3.3.2.3 Other chip select functions

The CS18 and CS19 chip selects are used to select the DACs U28A and U28B for programming the ADC offsets. CS20 and CS21 are used to set or reset a flip-flop, the output of which is used to enable or disable the bias supplies through a bank of analog switches. The CS22 in conjunction with the DO2-DO0 is used to generate ADC data buffer chip selects as shown in Table 3.4. CS23 is used to issue a reset command to ADC to self calibrate.

Table 3.4: Summary of ADC data buffer and other chip selects

Chip selects	Device	DO2-DO0	Function
CS 18	U28A	--	ADC offset
CS 19	U28B	--	ADC offset
CS 20	U32A	--	Enable bias
CS 21	U32A	--	Disable bias
CS 22	U15	000	ADC1 low byte
		001	ADC1 high byte
		010	ADC2 low byte
		011	ADC2 high byte
		100	ADC3 low byte
		101	ADC3 high byte
		110	ADC4 low byte
		111	ADC4 high byte
CS 23	--	--	Reset ADCs

3.3.3 Signal processing board

The signal processing chain implements various functions like DC offset removal, pre-amplification, double correlated sampling, bias offset and digitization of the signal. The CCD source follower (Figure 3.7) provides a constant current source. The current through the output FET can be controlled by VGMOS bias voltage. By adjusting the VGMOS to about 7.2V, an operating current of 40 μA is set through the output FET. The VSA is fixed at 5.5V. A block diagram of the signal processing chain along with the associated timing is shown in Figure3.8 while the schematic circuit is shown in Figure 3.9. The CCD signal is capacitively coupled to the pre-amplifier (U60) to remove the DC component from the signal. The pre-amplifier can have two selectable gains using SPDT (U62A). After pre-amplification, the signal is subjected to double correlated sampling (DCS) in order to eliminate the reset noise. The op-amp (U59) can be configured to +/- 1 gain using an analog switch (U61) that changes polarity depending on the state of SBIT11. When the SBIT11 is low, the U59 is configured as non-inverting unity gain and when SBIT is high, it is configured as inverting unity gain amplifier. The integrator (U40) integrates the input signal when SBIT12 is held low and holds the output when SBIT12 is high. The integrator can be reset by closing the analog switch (U42A, SBIT13 low) across the integrator capacitor.

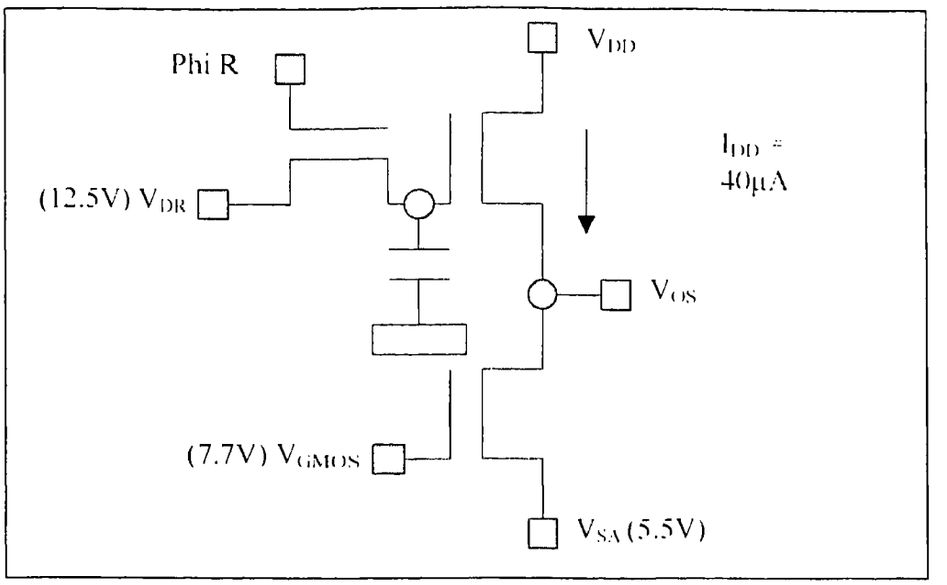


Figure 3.7: Schematic of THX7897M amplifier

3.3.3.1 Double correlated sampling and reset noise elimination

To measure the charge collected under each pixel, the output node capacitor is pre-charged to a reference voltage (VRD) by turning on the internal reset transistor. The thermal agitation of electrons in the reset transistor causes a certain uncertainty in the mean value of the final reset voltage on the capacitor. This uncertainty in the final voltage causes the reset noise and is given by $\sqrt{(kT/C)}$ volts where k is the Boltzman constant, T is absolute temperature and C is the node capacitance. The DCS technique eliminates this reset noise by taking two samples of the CCD signal per pixel, one before and one after the charge packet is shifted to the node capacitor. The reference signal is positively integrated (SBIT11 low) for a defined period of time (SBIT12 low) and after the charge shift, the signal is negatively integrated (SBIT11 high) for the same time. The resulting output at the integrator is proportional to the detected signal and is free from the reset noise. The integration also smoothens high frequency noise. The integrator has been configured for a gain of 1 microsecond. The DCS integration time and thereby the integrator gain can be varied using the state bit (SBIT12) of the signal processing control bits.

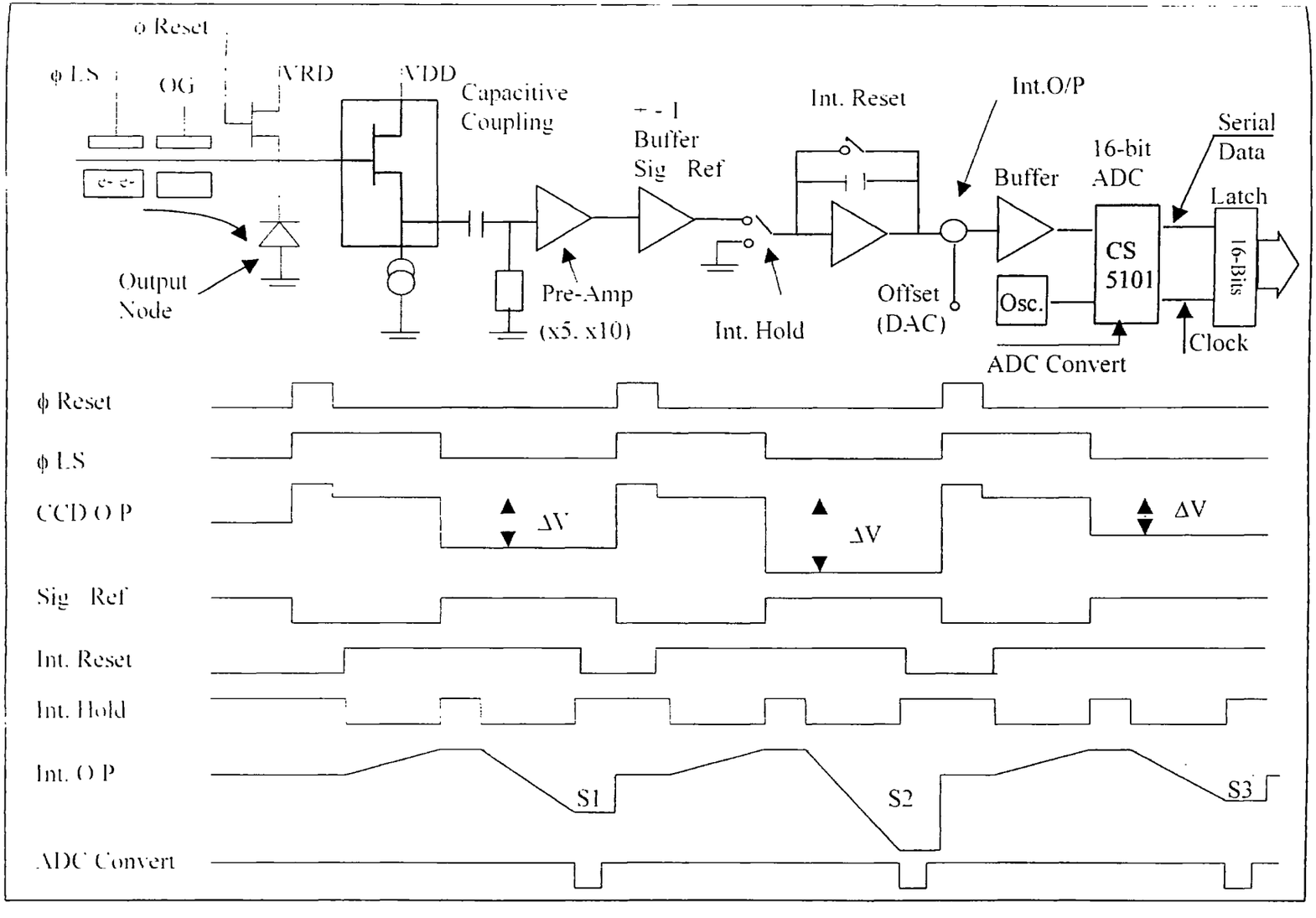
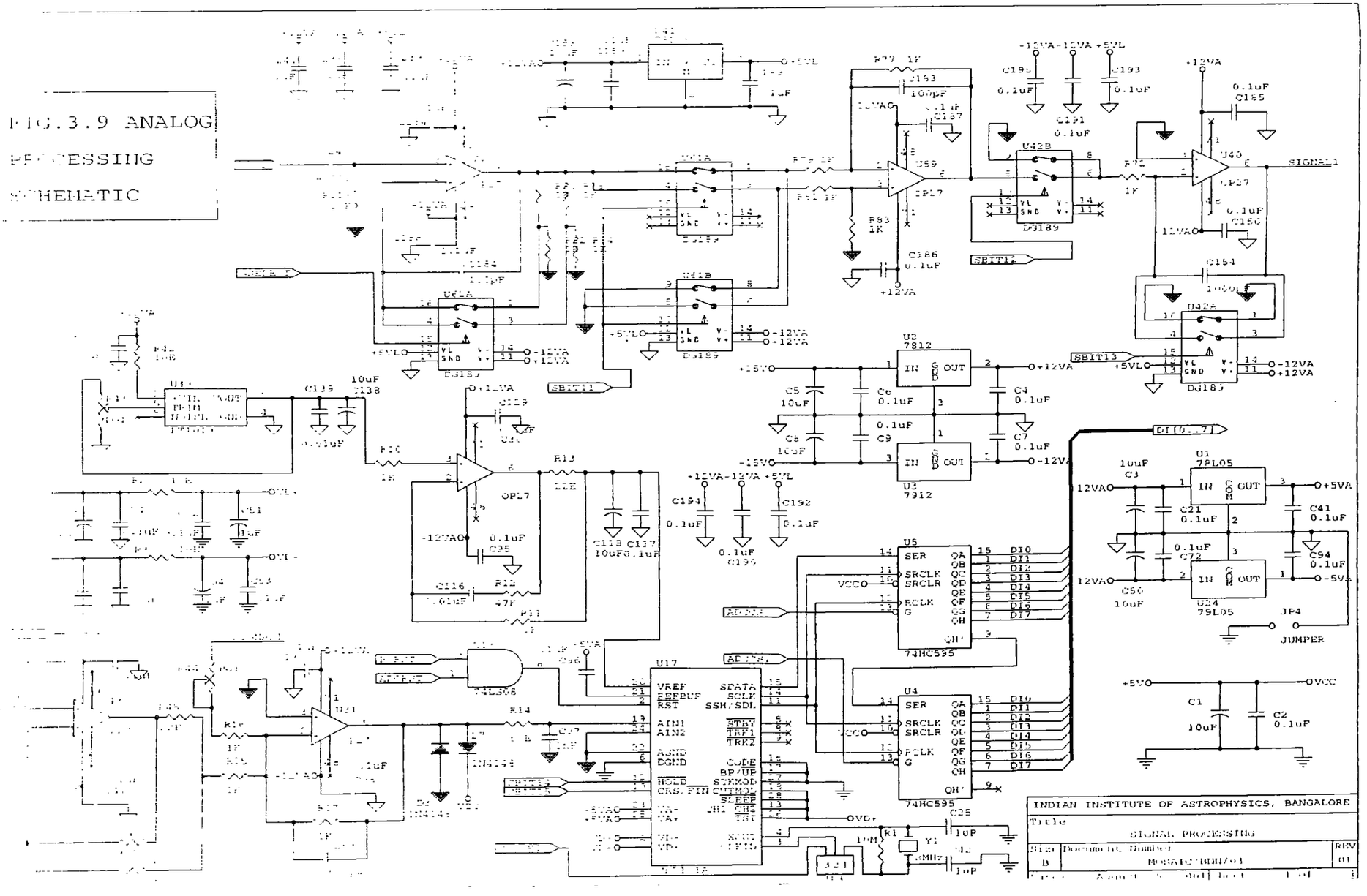


Fig.3. 8: Block diagram of video processing board and its timings

FIG.3.9 ANALOG PROCESSING SCHEMATIC



3.3.3.2 ADC and offset buffer

A 16 bit ADC - CS5101A - is used to digitize the processed signal. The CS5101A consists of a two channel multiplexer and a sampling device. The conversion time is 8uS and the digitized data is output in a serial form. Auto-zeroing capability of the device enhances power supply rejection at frequencies well below the conversion rate. The ADC is configured in unipolar mode and the code output is in binary format with a range of 0 to 65535. The ADC is operated in self-synchronous clocking mode to clock the 16 bit serial data into a set of shift registers (U4, U5). A low going pulse on SBIT14 triggers the ADC for conversion. The shift registers provide tri-stated outputs and permit connection to a common 8-bit data bus on the backplane. A buffer is used before the ADC, which presents low impedance to the sample and hold of the ADC. The integrator output is added with a suitable offset at U31 to ensure a positive voltages at the ADC input. An anti-aliasing filter at the output the buffer ensures that the ADC doesn't see any high frequency noise caused by the buffer.

Four such signal processing chains are implemented in a single 6 layer PCB, to process in parallel the 4 outputs of a single CCD. The control signals for these signal-processing chains are derived from the bias & clocks PCB as already explained. The DSP enables one shift register (8 bits) at a time and strobes the data onto the host interface card.

3.3.4 Host interface card

The host computer communicates with the DSP in the CCD controller through an asynchronous serial communication incorporated in a custom built ISA interface card. The block diagram of the interface card is shown in Figure 3.10 and the schematic circuit is shown in Figure 3.11. This interface board uses a Universal Synchronous Asynchronous Receiver Transmitter (USART, 8251) to communicate with the DSP, and a set of FIFOs (2 x 8K size) in aiding the data transfer from the controller. The board conforms to the 16-bit ISA architecture and supports the 8-bit data operations as required in the USART and programmable interval timer (8254) interfaces. The board can be configured in the address range from 200H – 3FFH. The DSP code developed with the assembler ASM56000 is down loaded (bootstrapped) from the host computer through the serial link. The host computer also handshakes with the DSP to ensure that the

commands sent are received properly. The DSP strobes the digitized data into the host interface board one byte at a time on a parallel port. Each strobe pulse (low) toggles the flip-flop U11 and the write pulses for the low byte FIFO (U22) and the high byte FIFO (U27) are generated alternately. The low bytes of every data point is written into U22 while the high bytes are written into U27. The U22 and U27 are cascaded to form the 16-bit data. The FIFOs status flags (empty, half-full and full) can be monitored through U5 for the progress in the data transfer. These FIFOs form the timing buffer between the received data by the host and transmitted data by the DSP.

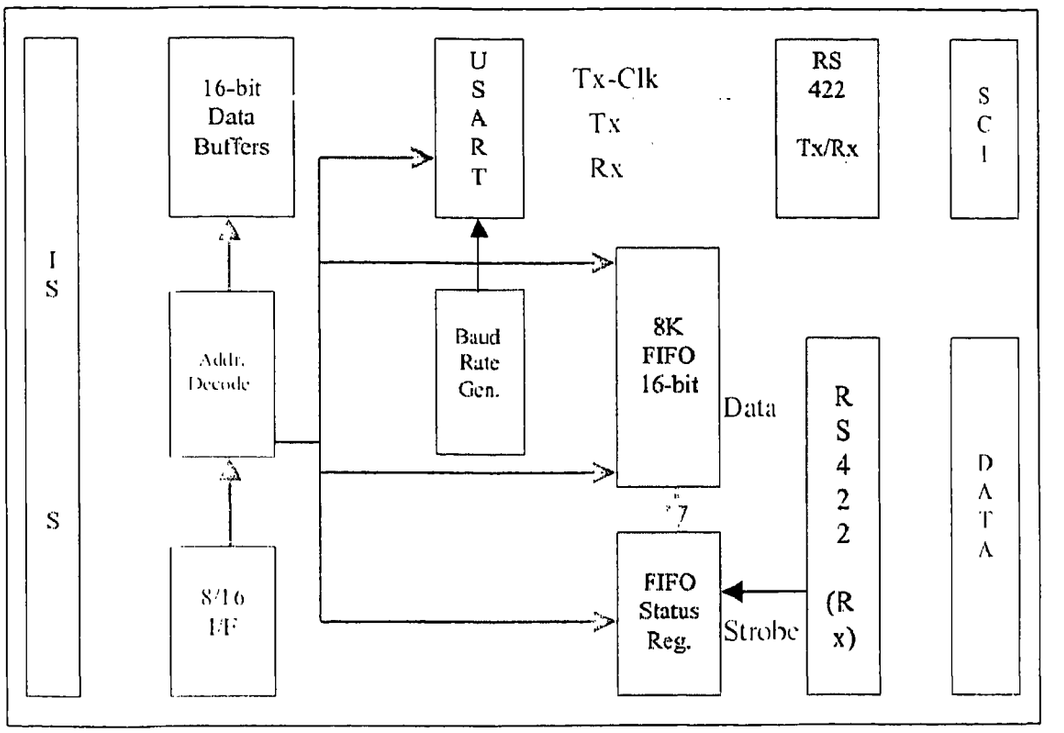


Figure 3.10: Block diagram of host interface board

The 8254 (U25) is used to generate the required clock frequency (16 times the baud rate). The USART (U17) also needs a clock 30 times greater than the baud rate for its internal operation. This clock is also derived from U25. The DSP56002 supports a baud rate of 9600 over its SCI. The USART is programmed with the same baud rate, character length, number of stop bits and parity as the SCI controller.

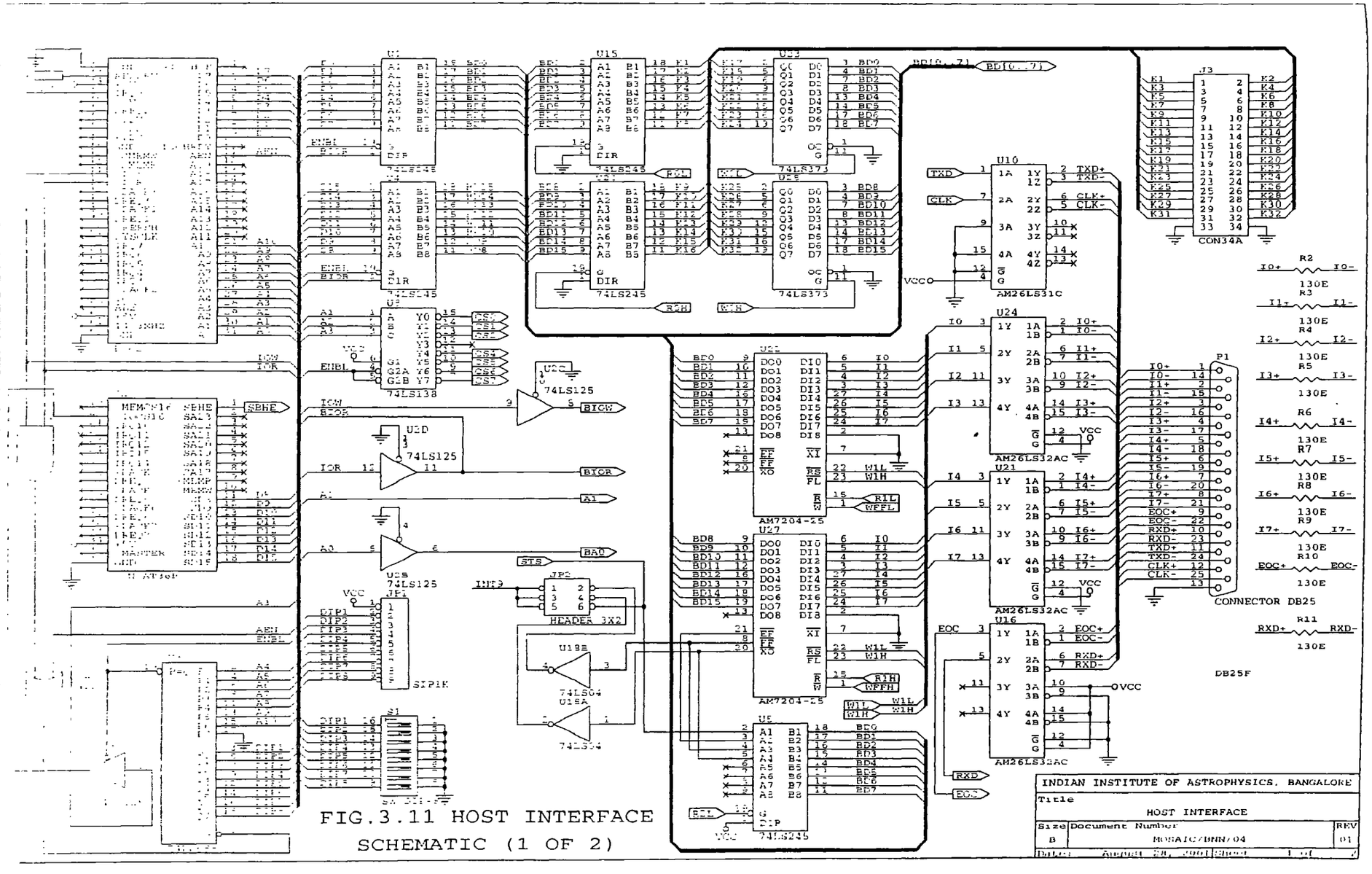


FIG.3.11 HOST INTERFACE SCHEMATIC (1 OF 2)

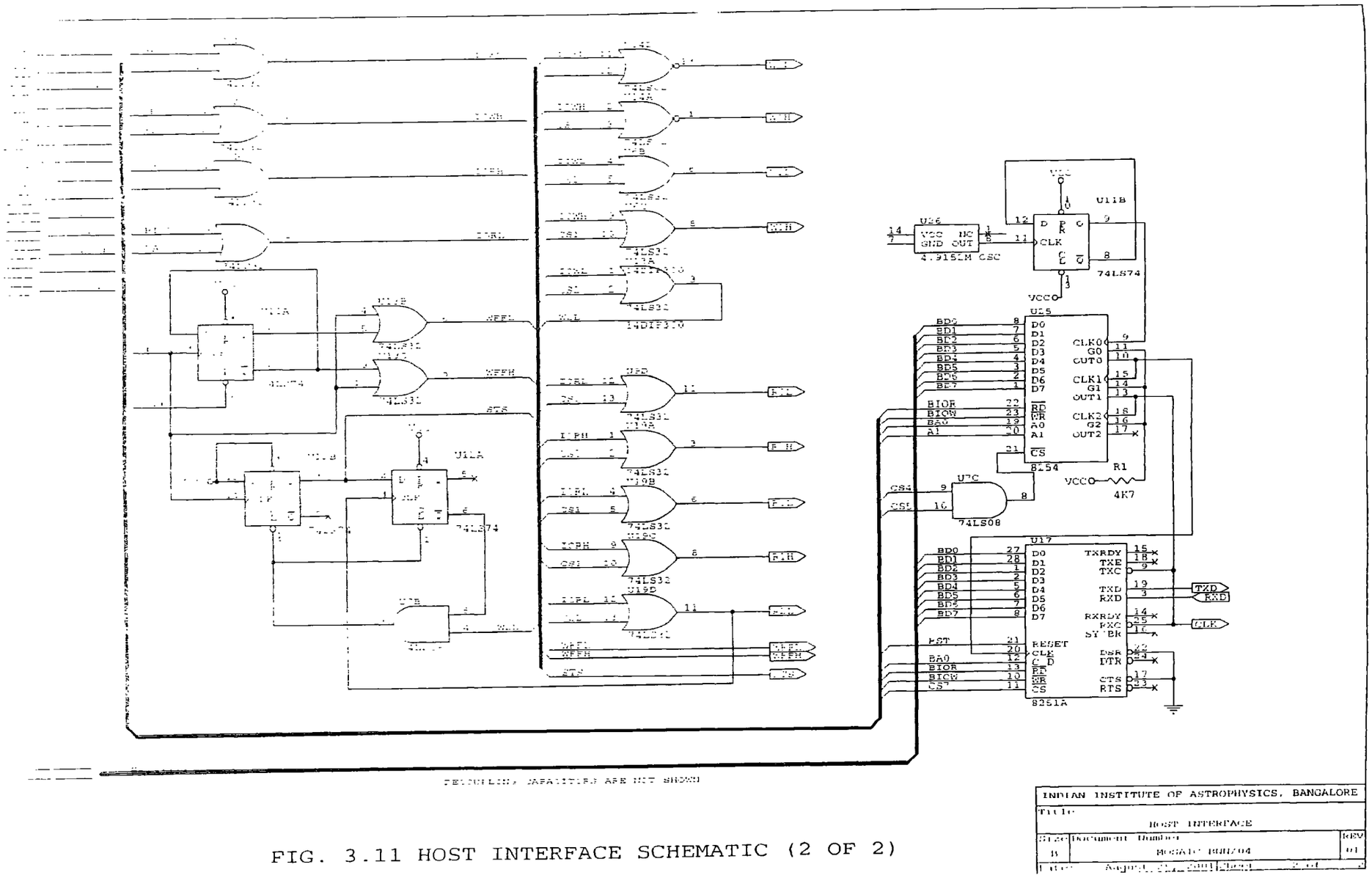


FIG. 3.11 HOST INTERFACE SCHEMATIC (2 OF 2)

3.3.4.1 Bootstrap loading

The host uses the DSP's SCI for the bootstrap loading of the program memory. This interface uses transmit data (Tx), receive data (Rx) and SCI serial clock (SCLK). The SCI is configured to use an external serial clock for the SCI communication. The SCI serial clock is generated in the host interface card. A hardware or software reset puts the DSP in the controller into the SCI mode. During reset, the bootstrap code of the DSP executes the SCI loading routine (list in appendix) to load its program RAM. This code expects 3 bytes specifying the number of program words, 3 bytes specifying the starting address of the Program memory and subsequently 3 bytes for each program word to be loaded. The words are received LS byte first followed by Middle byte and then the MS byte. After receiving the program words, the program execution starts at the address where the first instruction is loaded. Each byte, when received, is echoed back through the SCI transmitter.

3.3.4.2 Bootstrap code

The DSP assembler (ASM56000, DOS application) generates a formatted file called load file (a file with extension LOD) when assembled. This file is an ASCII file that can be read to pick up the program address and the code to be loaded into DSP. A host utility reads the LOD format file and converts it into a binary format suitable for the DSP controller. Once the DSP is loaded with the bootstrapping code, the DSP executes the program from the starting location in the program memory. The program then waits in a loop to receive serial commands from the host computer. The serial commands are of 24-bits width and when a command is received, the DSP acknowledges the host by sending a pattern 'AA' back to the host after execution of the command.

3.3.5 DC power supply

The controller is powered up by four DC linear power supplies 5V (5A), ±15V (3A) and 30V(0.5A). The DC power supply modules are specified for low ripple (5mV peak-peak) with short circuit and overload protection and have low EMI/RFI noise levels. The ±15V dual power supply is designed to be free from the common-mode latch up during power on. These power supplies are housed in a separate box.

3.4 Waveform editor

The OrCAD Schematic design tools (SDT386) are used to edit the waveforms. The schematic contains the levels of 16 state bits (state field) at any given time. The patterns are time-sliced and a time field (delay between states) is then combined with the state field to produce a combined word (24 bits). Sequences of such words are used to represent the parallel transfer, serial transfer or pre-flush waveforms. These words are inserted in the DSP assembly program in the waveform generation sub-routines. As an example a schematic entry for the serial transfer waveform for THX7897 device is shown in the Figure 3.12. The timing consists of 5 parallel, 5 serial and a reset clock control bits. The signal processing chain requires 5 control bits to implement the double correlated sampling technique. These control bits are set on the D15-D0 data bits of the DSP.

3.5. Configuring the controller

3.5.1 Steps involved

The controller needs to be programmed before any operations can be performed. The camera configuration involves the following steps / procedures.

- Read the current DSP code load file (*.LOD) to the system memory and create the bootstrap code from the load file. The assembly language program for operating the mosaic CCD, the LOD file format and the bootstrap code are listed in Appendix B
- Program the baud rate generator (8254, counter-0 and counter-1) to generate the required clock for the USART and the SCI, initialize the USART and program the serial communication parameters as described earlier. Send the bootstrap code a byte at a time to the SCI and compare with the byte received at the USART (echoed by the DSP) to confirm an error free bootstrapping.
- Once the DSP is bootstrapped, the DSP will wait to listen to the host commands.
- Program all the bias voltages, clock voltage levels and the ADC offset voltages in the controller through suitable host commands. Enable the bias voltages through a host command.

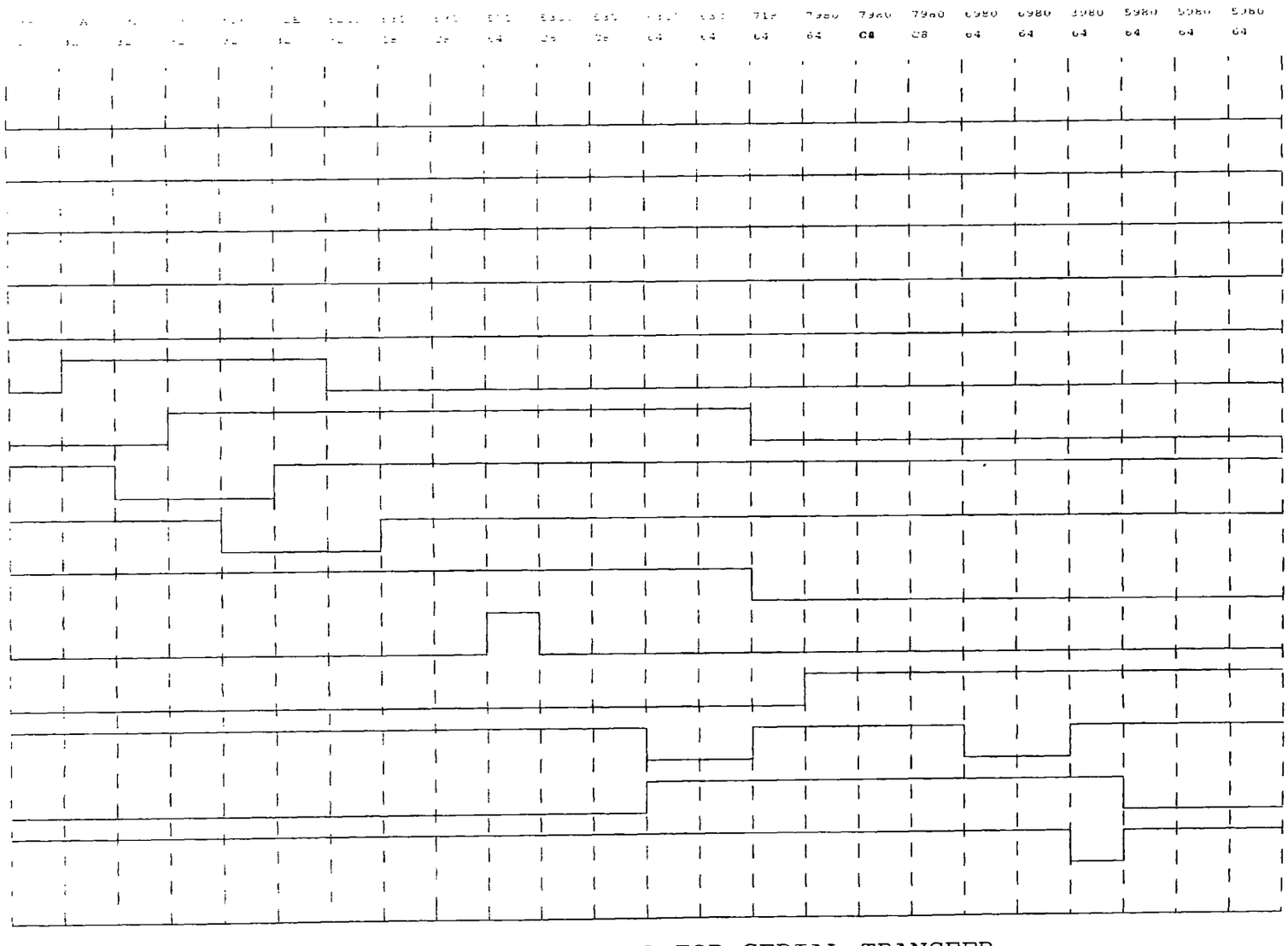


FIG. 3.12 TIMING FOR SERIAL TRANSFER

3.5.2 Host commands to the controller

The DSP listens to the host commands on the serial communication port. The commands are of 24-bit width and are identified by the DSP depending on the bit set in the most significant byte (C23-C16). The following commands have been implemented.

- LoadDAC: If the C16 bit is set, then the program execution jumps to LoadDAC sub-routine. A bias and clock board is selected using C15-C13 bits, while a particular DAC is selected by C12-C8 bits. The selected DAC is programmed with an 8-bit data present on C7-C0 bits.
- OutData: If the C17 bit is set, then the data present on C15-C0 is latched onto the back plane.
- ClearRows: If the C18 bit is set, a number of rows indicated by C15-C0 are shifted without digitizing.
- SerialShift: If the C19 bit is set, a single serial shift is performed that implements DCS signal processing technique.
- Preflush: If the C21 bit is set, then the CCD parallel array is cleared of any accumulated charge.
- ReadRows: If the C22 bit is set, then number of rows indicated by C15-C0 rows are shifted and digitized. The digitized data is sent to the host interface card along with a strobe signal.
- ResetDSP: If the C23 bit set, then the DSP is reset to the bootstrapping mode. This software reset permits reloading of a different code from the host required while changing any timing.

3.6 The IIA mosaic CCD controller

Each CCD device in the mosaic requires a separate bias & clock PCB and a signal processing board. Figure 3.13 shows the mosaic controller architecture configured to control four CCDs. To implement a mosaic of 2x2 CCDs, four bias & clocks boards and four signal processing boards are required. The DSP board is common for all the CCDs. The 9 PCBs are plugged on to a thick back plane PCB. The base addresses on each bias & clock board are set uniquely. The back plane PCB is mounted on to a 6-EURO standard card frame, which holds all PCBs. The back plane PCB incorporates slide on

receptacles to accept DC power supply voltages. A suitable enclosure for this controller has been fabricated incorporating the 6-EURO standard card frame, panel meter to indicate the CCD mount temperature and a potentiometer dial to set the desired operating temperature. The back panel contains the DC power inlet, the shutter control signal connector, an instrument-cooling fan and the host interface & the CCD camera head connectors. While the bias and clock voltages for each CCD are independently programmable through software, the clocking sequence is common to all CCDs. A single serial transfer simultaneously processes and digitizes all 16 channel signals. The DSP then sequentially enables the low and high byte of each ADC's data buffers and generates a strobe signal to transfer the data into the host interface board.

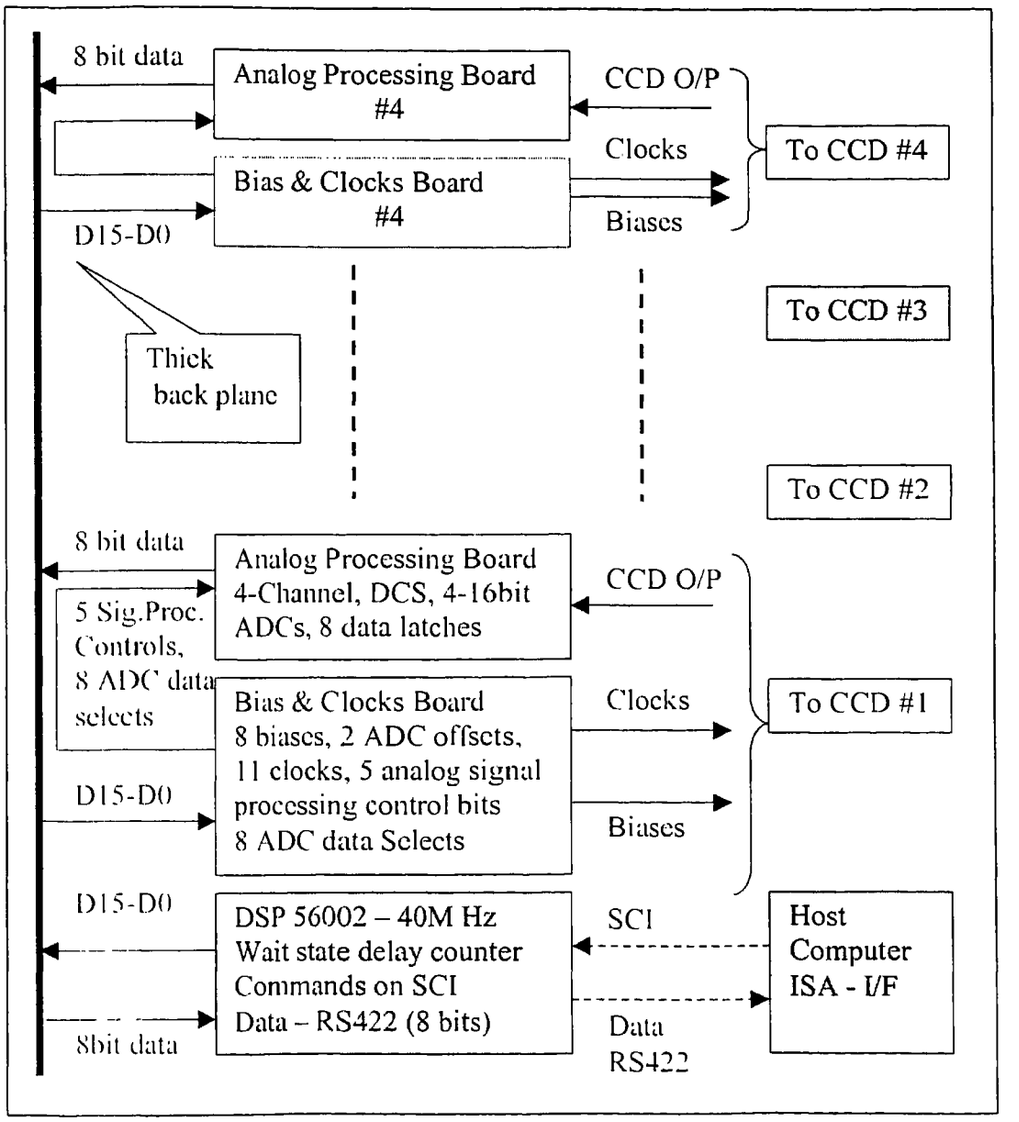


Figure 3.13: Mosaic CCD controller architecture

3.6.1 Specification of the mosaic CCD controller

Table 3.5 summarizes the specifications of the IIA mosaic CCD controller.

Table 3.5

Max. devices in Mosaic	4
Number of Readouts	16
Max. Pixel rate (per Readout)	50K pixels
Bits per Pixel	16
Bias Voltages	Fully programmable
Clock Voltages	Fully programmable
No. of Gains Selectable	2
Offset	Common for single CCD
Communication link	Serial, RS422
Data link	Parallel, 8bits
Host computer	PC/AT, ISA I/F
Controller noise	1.2 Counts

3.6.2 THX7897 bias and clock voltages

Tables 3.6 & 3.7 summarize the various bias and clock levels required to operate the THX7897 CCD.

Table 3.6: Bias voltages

Description	Symbol	Typical Voltages
Output Drain	VDD	+15V
Reset Drain	VRD	+13.5V
MOS Gate	VGMOS	+7.7V
Source Supply	VSA	+6.5V
Last Gate1	VGS1	0.5V
Last Gate2	VGS2	0.5V
Protection drain	PROT	+15V

Table 3.7: Clock voltages

Description	Symbol	Volts (low to high)
Parallel1	P1	-6V to +2V
Parallel2	P2	-8V to 0V
Parallel3	P3	-8V to 0V
Parallel4	P4	-8V to 0V
Transfer Gate	PS	-6V to +2V
Serial1	S1	-4V to +6V
Serial2	S2	-4V to +6V
Serial3	S3	-3V to +7V
Serial4	S4	-4V to +6V
Serial Sum	SW	-4V to +6V
Reset	ϕR	0V to +8V

3.6.3 Bias buffer units and crosstalk elimination

In the THX7897 CCD, each readout has separate VDD, VRD, VGMOS connections. Operating all the readouts from a single VDD, VRD and VGMOS poses crosstalk amongst the various readout channels. A four layer buffer-amplifier PCB has been developed, incorporating independent VDD, VRD and VGMOS bias supplies. The PCB also incorporates pre-amplifiers for the readout sections. These buffered bias voltages effectively eliminated the cross coupling of signals from any channel to the other channels. Four such PCBs, have been used for the mosaic of 2x2 CCDs. These PCBs are enclosed in a compact box which is mounted on the cryostat.

3.7 Configuration for other CCDs

To demonstrate the programmable features of the CCD controller, 2 more CCDs were tested. Two more units of this controller have been built, one for a 2K x 4K (ST002AB) CCD and another for a 2K x 2K (SI424) CCD from SITe. The ST002AB is a dual readout device while SI424 is a single readout (other readouts non-functional) one. Each controller utilizes one DSP CPU board, one clocks & bias board and one analog processing board. The high VOD voltages that are required by the ST002AB and SI424 and other bias & clock voltages could be generated in the controller. For the SI424 device, a four layers PCB is used inside the cryostat which provides passive filtering on the clock & bias voltages and incorporates a pre-amplifier to drive the output signal to the CCD controller. Table 3.8 and Table 3.9 list the bias and clock voltages generated for the ST002AB and SI424 CCDs respectively.

Table 3.8: Bias and clock voltages for ST002AB

Bias voltages		Clock voltages	
Description	Volts (V)	Description	Volts (low to high)
Output drain (a)	25.0	Parallel 1, 2	-9.0 to 2.5
Reset drain (a)	15.0	Parallel 3	-7.0 to 6.0
Overflow drain	20.0	Serial 1, 2, 3	-6.0 to 5.0
Last gate (a)	-4.0	Sum well	-6.0 to 5.0
Output drain (b)	25.0	Reset gate	0 to 12.0
Reset drain (b)	15.0		
Last gate (b)	-4.0		

Table 3.9: Bias and clock voltages for SI424

Bias voltages		Clock voltages	
Description	Volts (V)	Description	Volts (low to high)
Output drain	25.5	Parallel 1, 2	-8.5 to 4.5
Reset drain (a)	13.4	Parallel 3	-8.5 to 7.5
Last gate	-3.5	Serial 1, 2, 3	-5.0 to 7.0
Drain protection	-9.0	Sum well	-4.0 to 7.0
		Transfer gate	-6.0 to 7.0
		Reset gate	0 to 12

3.8 Hardware based data compression

Since the mosaic CCD camera systems produce large amount of data it was considered fit to expedite some of the compression techniques and arrive at a suitable method. In the context of remote operation, the compression of data on-line decreases the effective data bandwidth required in image transmission. Hardware data compression is preferred for the on-line data over the software compression techniques since the host is left free to handle other chores while the compression is done by an independent hardware.

We considered using a high-performance Adaptive Loss-less Data Compression (ALDC) processor, ALDC1-20S-HA, from IBM for online image data compression in our controller. The ALDC implements LZ compression algorithm (Ziv, J., and Lampel, A, 1977, 1978) and operates at 20MB/s. We added the ALDC1-20S to the host interface card of the CCD controller and evaluated the performance of the ALDC (Naidu and Srinivasan, 2001).

3.8.1 Functional units of ALDC

The main functional units of the ALDC are shown in Figure 3.14 and comprise of encoder and decoder circuits, a microprocessor interface, Original Data Interface (ODI), and Compressed Data Interface (CDI) The ALDC encoder accepts data bytes from the ODI and provides compressed data to the CDI. The ALDC decoder accepts compressed data bytes from the CDI and provides the reconstructed data bytes to the ODI. The encoder and decoder contain a 512-byte history buffer for performing the compression and decompression operations.

3.8.1.1 ALDC registers

The ALDC has several registers to configure and perform the data compression and decompression operations (ALDC Design notes, 1994). The status register (STAT) indicates the current status of the data transfer. The ODI configuration (OCNF) and the CDI configuration (CCNF) registers configure the ODI and CDI ports using the Command (CMND) register. The CMND register is used to trigger the ALDC to commence the compression or decompression operation, program the ODI and CDI ports, set compression / decompression bypass etc. The ODI transfer count (TCO) and the CDI transfer count (TCC) registers provide the status information on the number of bytes transferred through them. The transfer count register (XFR) is used to program the data transfer size used in compression or decompression.

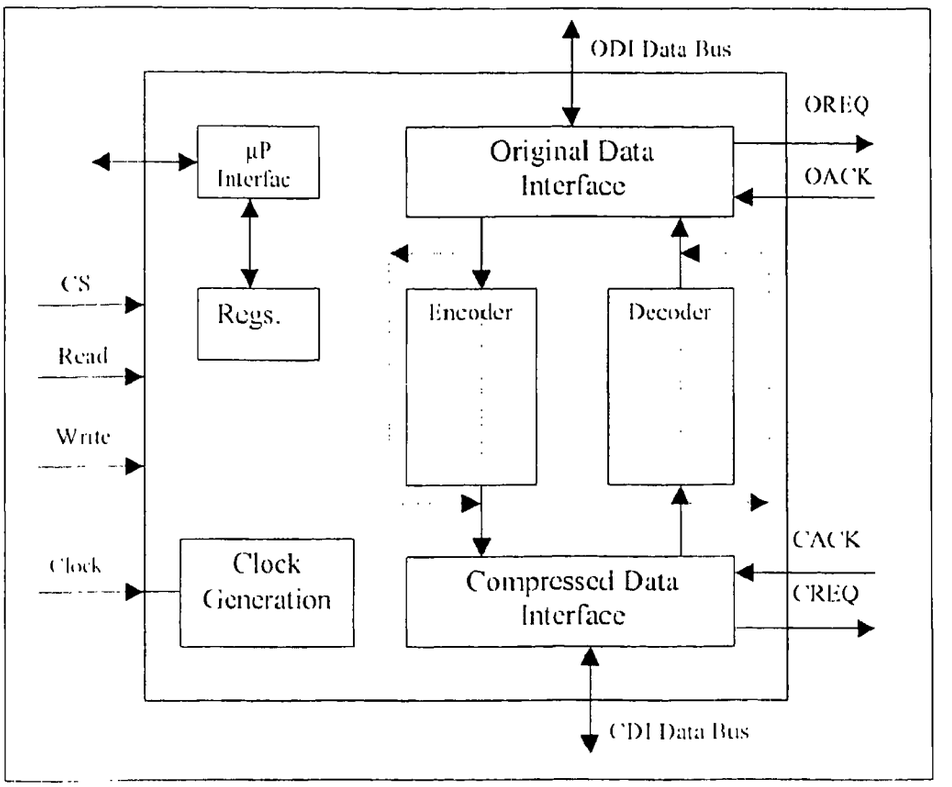


Figure 3.14: Functional block diagram of ALDC.

3.8.1.2 Data transfer

The data transfer starts with a request asserted by the ODI to initiate the data transfer. Acknowledge signal should be asserted in response to the request, which leads to a withdrawal of request. When the acknowledge is withdrawn, the data is transferred into the ALDC. There can be multiple acknowledges and data transfers for a single extended request. The data transfer operations typically involve blocks of data bytes with fixed or variable length. The transfer size (in bytes) is loaded into the XFR register. The OCNF/CCNF registers are programmed with a FIFO threshold and the CMND register is used to trigger the data compression / decompression. The transfer proceeds until the specified numbers of bytes are processed. During the processing, the compressed / decompressed data is output on CDI / ODI as it becomes available.

3.8.2 Interface description

The block diagram of the hardware interface of the data acquisition card to the ISA bus is shown in Figure 3.15. During the compression, the ALDC asserts OREQ signal. Acknowledge signal (OACK) is generated in response to this assertion, by a write operation on ODI or a read operation on FIFOs (on-line CCD data). This operation allows either the data from memory or the on-line data from FIFOs to be transferred on to ODI for compression. When the compressed data is available, the ALDC asserts CREQ signal. An acknowledge signal CACK is generated in response to this assertion, by a read operation on the CDI to read the compressed data. During decompression, the ALDC asserts CREQ signal. The acknowledge signal CACK is generated in response to this assertion, by a write operation on the CDI with data. When the original data becomes ready, the ALDC asserts the OREQ signal. An acknowledge signal OACK is generated in response to this assertion, by a read operation on the ODI to read the original data.

3.8.3 Software description

The compression / decompression function of the ALDC has been checked using the disk files. The software involved in these operations is described below and flowchart is shown in Figure 3.16.

For compression, a software reset is issued initially to the ALDC by programming the CMND register. Then XFR register is loaded with the size of the file to be compressed. The OCNF register is programmed with a suitable threshold and burst mode of operation. Then the CMND register is programmed to trigger the compression operation. The program now checks the status of ODI to see if OREQ is asserted. When ODI is ready to accept data (OREQ is asserted) the program reads a block of data from the input file and transfers to ODI a byte / word at a time. After transferring each data, the program checks the status of the CDI to see if any compressed data is available. If the CDI is ready with data (CREQ asserted), the compressed data is read from the CDI and stored in the output memory block. After compressing an input block of data, the output data is stored onto an output file. The process is repeated until the whole input data is processed.

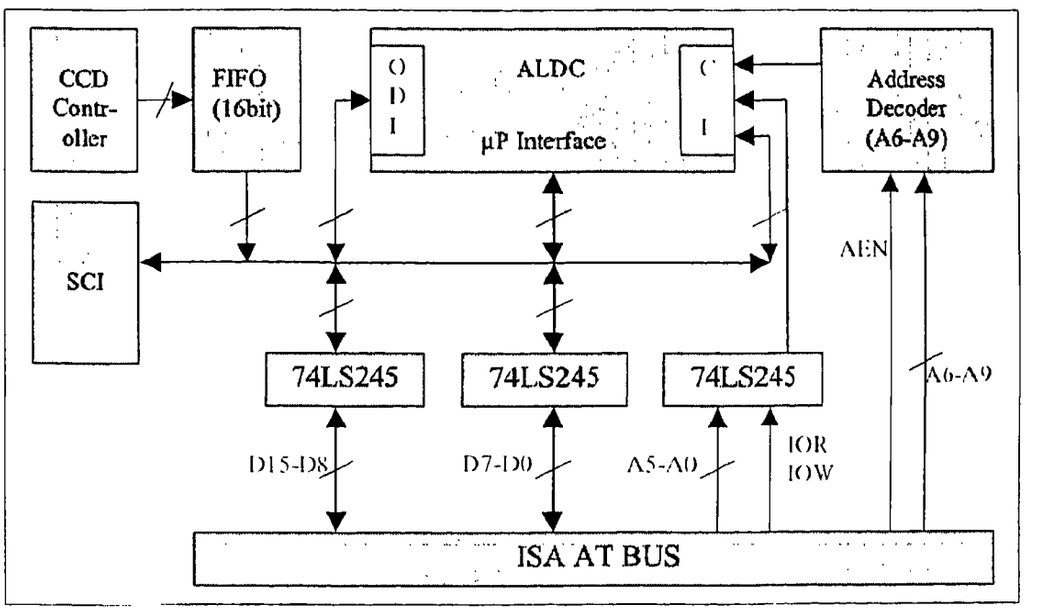


Figure 3.15: Block diagram of the ALDC interface.

For decompressing the compressed files, the XFR register is loaded with the size of the compressed file. The CCNF register is programmed with a threshold and burst mode of operation. The CMND register is then programmed to trigger the decompression operation. The program waits in a loop checking the status of the CDI, and transfers the file one block at a time when the CDI is ready (CREQ is asserted). During this block

transfer, the program also checks the status of the ODI. When the ODI is ready, the original data is read from the ODI and the compressed data is stored in an output file.

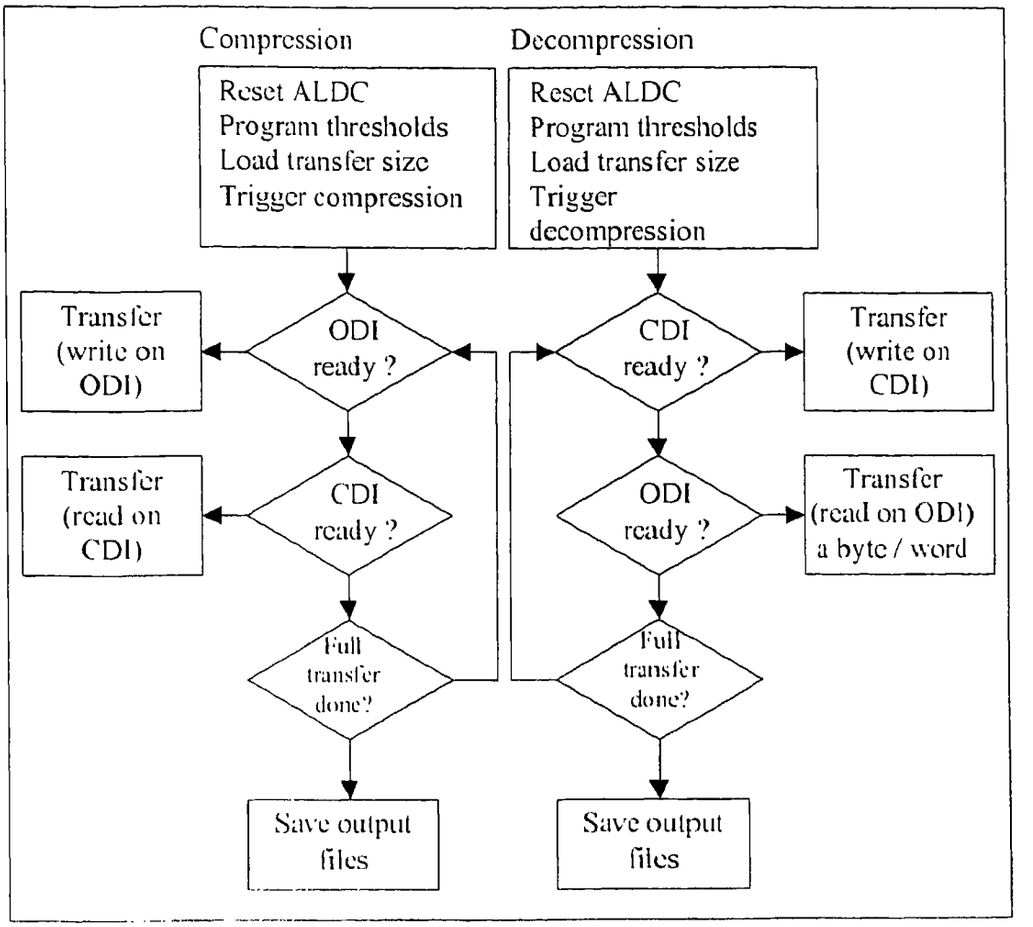


Figure 3.16: Flowchart for data compression and decompression.

Table 3.10: Summary of hardware data compression

File Type	Original Size	Compressed Size		
		Method Of Compression		
		ALDC	PKZIP*	COMPRESS**
Binary	449,280	255,138	167,457	272,922
ASCII	168,790	21,390	14,876	26,665

* PKZIP PKZIP.EXE Version 2.04G. PKWARE, 1993.
** COMPRESS Microsoft File Compression Utility. Version 2.00. 1992.

3.8.4 ALDC performance

An average compression factor (compressed/original) of 0.75 and 0.15 has been achieved for the binary and ASCII files respectively. The compression performance is comparable with the PKZIP and COMPRESS software utilities. Table-1 summarizes the performance of the ALDC hardware data compression.

3.9 Performance summary

The gain for all channels has been set to 3.85 e⁻/ADU. The controller gives a noise count of 1.2 when the signal inputs are grounded at the dewar connector end. A detailed performance of the controller is covered later in chapter 5.

Chapter 4

Data acquisition and display software

4.1 Introduction

The growth of large format CCDs puts new demands both on the CCD controller hardware and acquisition software designs. As the CCDs become large, the size of the data to be handled increases and higher computing power is needed in order to process the data. The CCD acquisition software has undergone rapid developments with the advent of computer hardware and operating systems. In recent years, the Microsoft Windows has received keen user attention due to its graphical user interface.

Initially, the CCD data acquisition and processing software was developed under Microsoft Windows 3.1 operating environment using Object-Pascal for windows. The software exploited the advantages of objects in providing custom specific tool boxes that implement the different functions of the CCD data acquisition and image processing (Naidu et al, 1997). The acquisition software was subsequently ported to Windows/9X/NT using Delphi Developer 2.0. In this chapter, the facilities and tools available for Windows programming and the advantages of programming in windows are presented. The modularity of the software structure and the various functions that are implemented are described. The flexibility of the software in handling different CCDs and mosaic arrangement is illustrated.

4.2 Why program under Windows ?

Windows offer several advantages to the programmers: 1) The graphics device interface (GDI) provided under the windows control insulates the application developer from the details of the output display device. The application simply outputs to the GDI and the Windows takes care of formatting, appropriate to the output device being configured. 2) The Event-Driven architecture allows windows to generate messages when an input event occurs and the messages are placed in a queue for appropriate actions. The application program at its convenience, reads and processes the messages. 3) Windows takes care of allocation and de-allocation of the memory for each application through its memory manager, using handles. Each object in the Windows program is identified by a handle. 4) The memory management under Windows lets more than one program to share the same module of compiled code using dynamic link libraries (DLL).

4.3 Programming for Windows

4.3.1 Object oriented programming

In Object Oriented Programming (OOP), the data structures are declared as object types which include procedures and functions that are needed in manipulating the data in the object itself. The two fundamental mechanisms that are used in this approach are encapsulation and inheritance. The basic concepts of OOP are described below.

4.3.1.1 Concepts of OOP

Objects: The fundamental concept of OOP is the Object. Objects are types of records/data structures that contain procedures and functions, called methods, to manipulate the data - an approach called encapsulation. So, an object is a self-contained unit. A new Object can inherit all the data fields and methods of a parent Object and its ancestor Objects - an approach called inheritance. New methods/features can also be added to the descendent Objects. Messages can be sent to Objects to tell them to carry out their built-in methods.

4.3.1.2 Advantages of OOP in Windows

The key to Windows programming is the Windows Application Programming Interface (API). Windows provide over 600 different API functions that an application can use. The Object Windows provide an easy way of using these API functions. Object Windows provide all the Window features and deal with the API directly. The programmer can concentrate on the core of the program while the most of the front-end functions are dealt by the Object Windows. Thus, the OOP provides valuable tools in reducing the amount of work required in complex programming projects. The Inheritance and Encapsulation features are extremely useful in managing the complexity. Added to that, the extensibility and reusability makes it an ideal tool for powerful programming. OOP provides a ready made frame work within which the programmer uses the objects to represent the user interface elements of a Windows program. The window and application objects manage the message processing behavior required for the Windows program, greatly simplifying the programmer's involvement in managing the application behaviour. These advantages lead to the development of a well behaved Windows program in much less time and with less effort compared to a non-window and standard structured environments.

4.3.1.3 OOP tools

Presently several compilers are available for OOP under Windows, like Borland C++, Turbo C++ for Windows etc., all of which have comparable features. However, for the programmers with a flare for Pascal, the choice is Borland's Pascal (BP) with objects. Delphi forms a good choice for Windows95/98 and Windows NT platforms. The following sections describe the object oriented design in Delphi and the implementation of the acquisition software using Delphi.

4.3.2 Object oriented design in Delphi

Delphi is an Object Pascal language developed for a visual programming environment. Delphi provides a comprehensive library of reusable components and supports two-way

design tools ie. modifying source files reflect in the visual tools and vice versa. Because Delphi runs in a 32-bit flat address space one could declare large data arrays as required for the mosaic CCDs. Components in Delphi, which are the building blocks of an application, are objects in the OOP sense. A component at its simplest form, is any object that is descended from *Tcomponent* which defines the basic behavior that all components must have. It can plug into the Delphi development environment and the users can use it in their application by modifying its properties and methods to suit the particular requirements during the design time. The most familiar attributes of a component are its properties, events and methods. The properties allow the user to set initial values at design time. The users can specify their own event handlers for the pre-defined events. The methods can be used to tell a component to perform a specific task. Delphi provides an object inspector to view and change the properties at design time in order to customize the components before running an application. Standard Delphi components have also encapsulated events for the common user actions such as mouse click etc.

Writing a graphic Windows application calls for the Graphics Device Interface. Delphi encapsulates the Windows GDI and provides a simple graphics interface called Canvas. The Canvas manages all those functions required with the GDI like getting a valid device context, creating, selecting and releasing handles etc. By caching the graphic resources, Delphi greatly speeds up repetitive operations. Delphi also provides components for handling bitmaps, icon etc which simplify the tasks for display of images.

4.4 Data acquisition software – the user interface design

4.4.1 Mainform

The data acquisition software contains a main form (*MainForm*), which provides the primary user interface. Figure 4.1 shows the *MainForm* at design time. Several other forms such as dialog boxes and secondary windows present input / output details. A few other components like *MainMenu*, *OpenDialog*, *SaveDialog*, *Timer*, *Panel*, *Image* etc, are dropped on to the *MainForm* from the component palette within the integrated development

environment (IDE) of Delphi. The user menu for the *MainForm* is designed using a menu designer through the *MainMenu* component. The *OpenDialog* and *SaveDialog* components are used to create a common Windows Open / Save dialog boxes that enable users to specify the name of a file to open / save. The

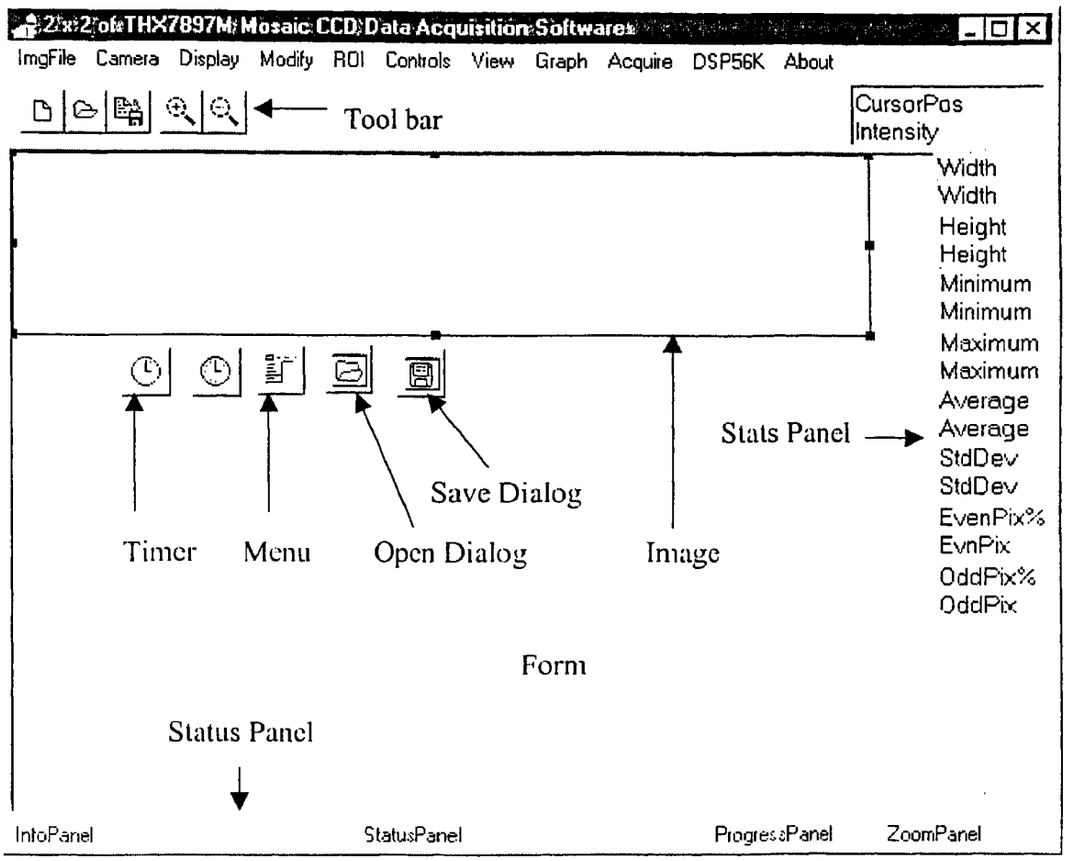


Figure 4.1: Mainform design using components

properties of these components have been used to specify a default file extension, a filter or mask to display a specified set of files and to set the current directory. The Timer component is used to set and track the exposure times. The Image component handles the bitmap image display, zoom and squeeze implementations. The picture property of Image component is set to bitmap. The *StatusBar* component is positioned horizontal and aligned along the bottom edge of the *MainForm*, to display the status information of the application. The Panels property of the *StatusBar* is used to add a collection of individual panels in the status bar.

each having its own text, width, style etc, to show the status information on various aspects. The InfoPanel shows the information / help on menu commands. The StatusPanel presents the status of the application and the ProgressPanel shows the exposure progress. The ZoomPanel shows the present zoom / squeeze factors with which the image is being displayed. These properties have been set at design-time, using the panel editor. The *SizeGrip* property is set to true to include a sizing grip at the right end of the status window which can be used to resize the *MainForm*. A tool bar is provided at the top of the *MainForm*, below the menu bar, which holds a few speed button components. The speed buttons represent shortcuts for certain menu commands. The *OnClick* events for these components have been attached to the respective menu commands. The *MainForm* also contains a panel to present the cursor coordinates and count values, and another panel to display statistical data of the image.

4.4.2 Dialog Boxes and secondary forms

The acquisition software uses several forms as dialog boxes for the user interaction to obtain detailed input and display information. There are two types of dialogs viz. modal and modeless. The modal dialogs do not allow the user to interact with the rest of the program until the dialog box is closed. A modeless allows the user to switch between the dialog and the rest of application. Dialog boxes which configure camera, set CCD Format parameters, bias, clock and ADC offset voltages are examples of modal dialogs while the Modify LUT dialog and plot forms are used as modeless dialogs. The input dialog boxes have been provided with a range checking facility. The program notifies any invalid or out of range values while leaving the input edit field to facilitate user corrections. A memo component has been used in a separate form to display the DSP bootstrapping code and its address locations. All these forms are referenced from the MainForm by including them in the Project.

4.4.3 Custom components / units

The acquisition program is modular and distributed over twenty units. Table 1 lists the units and their functions. Most of the units have their own forms. Some new objects like rFITS and wFITS have been developed as descendent from the TObject. The TObject contains constructor and destructor methods which allocates / disposes dynamic instances of the object in memory. Several properties have been added to get / set the FITS header information and data. The methods of these properties are coded in the implementation part of the units and permit access to the protected fields of the objects. In the main program, a variable of the object of type rFITS or wFITS can be created and the header information or the data can be read or written through the methods of the respective objects.

Table 4.1: Summary of various units and their functions

Unit name	Functions
About	Dialog to show software version etc.
ADCoffset	Dialog to program ADC offsets
CamConfig	Dialog to configure the camera
CCDFormat	Dialog to set readout parameters
DSPCode	Form to display DSP bootstrap code and address
Expose	Dialog to set exposure times
ImageInfo	Dialog provides image header information
Main	Form which provides main user interface
MCUnit	A unit deals with the hardware. acquire functions
ModifyLUT	Dialog to allow contrast stretching using LUT
Plot	Form to present graph
PlotLimits	Dialog to stretch plot limits
RFITS	A unit to read a disk FITS image
Scale	A dialog to set data scaling method
SetBias	A dialog used to program the bias voltages
SetClocks	A dialog used to program the clock voltages
Shutter	A dialog to test the shutter operations
Splash	A form that is displayed briefly before DAS
Stats	A unit to compute statistics of the image data
WFITS	A unit used to write FITS images to disk

The code relating to the camera control is implemented in a separate unit called MCUnit (Mosaic Controller Unit). This unit needed a custom component to provide access to the

system hardware. Delphi did not provide any functions / procedures to access the input output ports. We have selected a commercial component called TvicPort (Victor Ishikeev, 1997) in the MCUnit in order to access the hardware ports in the Windows95/98 or WindowsNT environment. The MCUnit implements methods to bootstrap the DSP, to send commands to the CCD controller and to acquire data. A ComDrive component (Cocco, 1997) has also been added to implement the filter-wheel automation through a RS-232 port. Sockets (Communication through network) have been added to the application which enables remote operation of the controller through socket messages.

4.5 Functions of the data acquisition software

The CCD Data Acquisition Software (DAS) program has been developed to operate under the Microsoft Windows98/NT environment. The features that are built into the software are: image acquisition, image display, image analysis, file operations, a few engineering functions and some utility functions. Figure 4.2 shows the main user interface window during the run time.

4.5.1 Camera functions

The software is designed to be a general purpose one which can operate different CCDs. The 'CCD Parameters' dialog box (Figure 4.3) enables the user to set the binning, sub-array readout and pre-flush count. The acquire functions set acquisition of bias, dark or image frames with a selection of exposure times. The acquired image will be displayed in the image window. The progress status panel bar shows the exposure progress continuously. The exposures can be aborted at any time before its completion. The acquired data can be saved either in 16 bit FITS or 8 bit bitmap format.

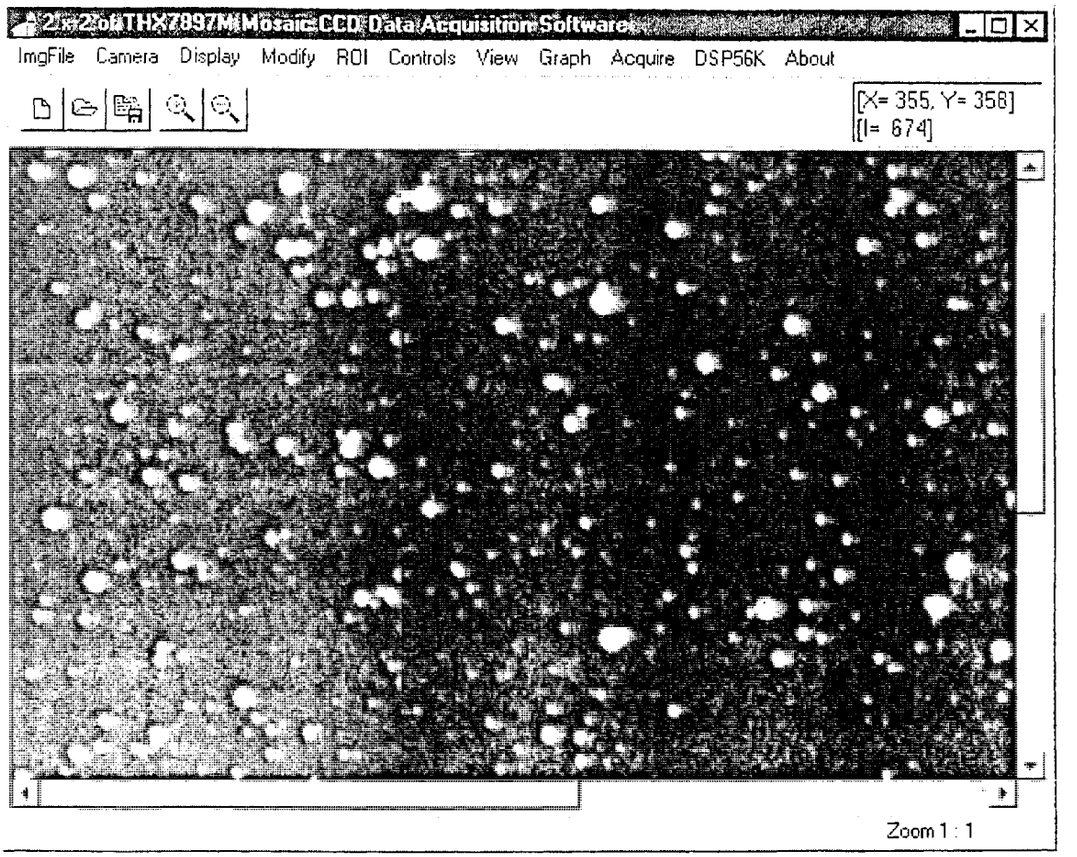


Figure 4.2: Main window at run time

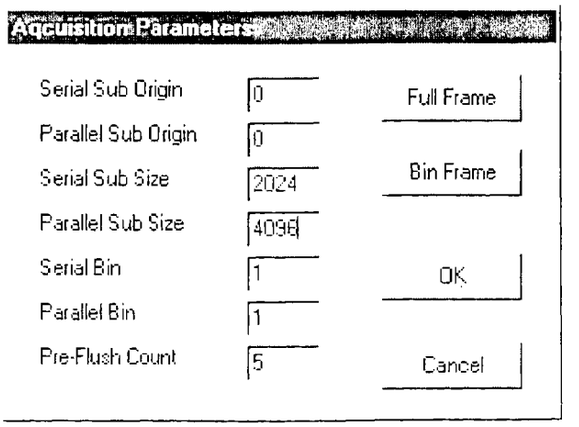


Figure 4.3: CCD acquisition parameters dialog box

4.5.2 Image display

The image display functions address both the display of CCD images as they are readout as well as the stored (16 bit FITS or 8 bit bitmap format) images. The display functions enable the user to select a method to convert the image pixels to screen pixels and zoom, squeeze the image.

4.5.2.1 Scaling methods

The image pixel values acquired from the camera controller are of 16 bit depth. For display purposes, the most significant 7 bits in the processed data are used leading to 128 gray levels. Although, the commonly available display drivers support 256 color levels, the system itself reserves 20 entries for its own use (Jeff Prosise, 1995). The gray levels are obtained by programming the red, green and blue colors with equal intensities. A few scaling methods have been implemented to translate the image data into image display indices (Figure 4.4). The linear scaling method implements a linear function to display all the pixels between minimum and maximum pixel values. This is the default method by which any newly acquired image is displayed. This method is not suitable in images where most of the useful data lie at low counts in the presence of some extraneous noise. A histogram equalization method has been implemented which computes the image histogram to determine a non-linear function in optimizing the image contrast. Basically, all the input pixel intensities are mapped in such a way to produce an output intensity histogram that is as flat as possible (Gonzalege and Wintz, 1977). This method brings up the low level features prominently. A fixed min/max method allows the user to stretch the image between selected minimum and maximum values.

4.5.2.2 Intensity mapping

In another method of image display, the user can interactively change the mapping between the pixel values and the gray palette. The 'Change Monochrome LUT' dialog (Figure 4.5), shows a few mapping modes. For linear mapping, the slope of this transfer function can be

changed by setting the minimum and maximum gray level index using the bottom and top scroll bars. An increase in the slope increases the contrast between adjacent intensity levels. By changing the top and bottom indices and retaining the slope, the user can achieve a desired contrast stretching through the data range.

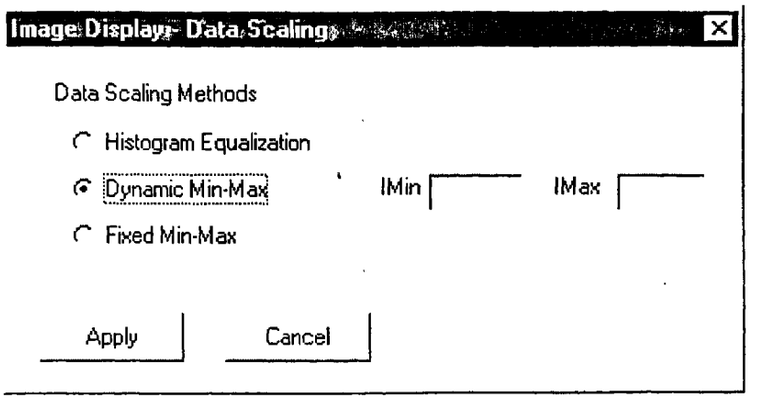


Figure 4.4: Display scaling methods

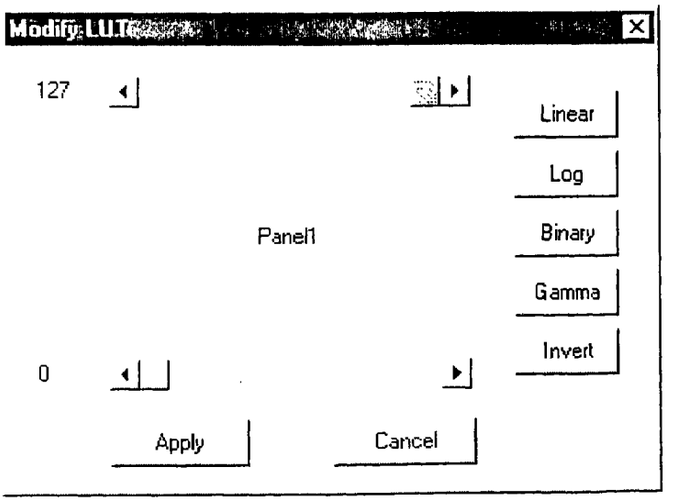


Figure 4.5: Change monochrome Look-up tables (LUT)

4.5.3 Analysis functions

The row, column and line plots display the pixel intensities along a straight line while a histogram plot shows the pixel intensity distribution in the image. Stretching the plot-limits on the X or Y axis permits a close look at the data in the selected regions. The stats panel

presents some basic image statistics like image minimum and maximum, average and standard deviation, number of odd and even pixels etc. The cursor panel shows the image coordinate and corresponding intensity counts associated with the mouse pointer in the image region. The acquisition, display and analysis functions can also be operated in a region of interest.

4.5.4 Filter selection

An user interface has been developed for selecting and positioning the filter-wheel and is shown in Figure 4.6. The filter-wheel unit has three wheels, with each wheel accommodating 6 positions (5 filters + 1 clear). Whenever a filter in a wheel is selected for positioning, the other two filter-wheels are moved to their clear positions. Since no absolute encoders exist to decode the filter position, a home position is sought every time before positioning a new filter. The filter names are entered in the in the standard initialization (filter.ini) file according to their positions in each wheel. The filter-wheel drive is configured for COM port. The program uses a ComDrive component to initialize a serial port and allows the user to set the serial communication parameters (Figure 4.7) and communicate with the drive.

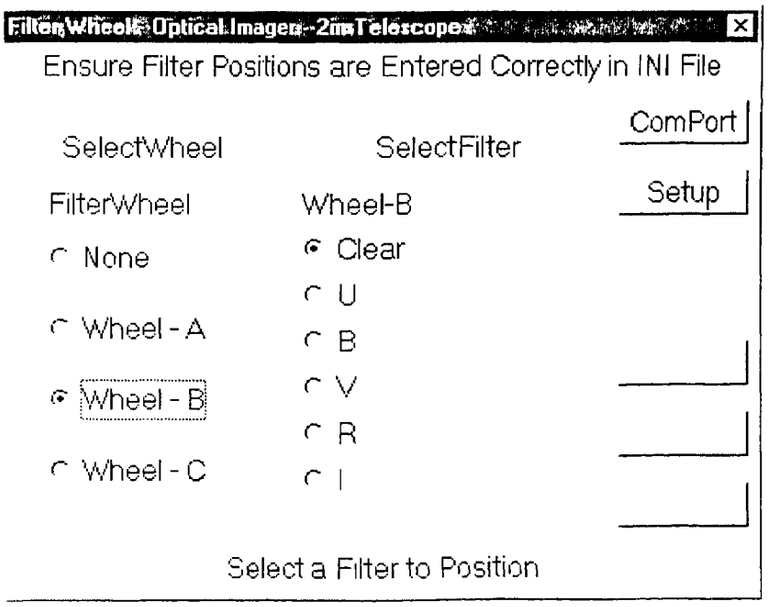


Figure 4.6: Graphical user interface for filter-wheel operation

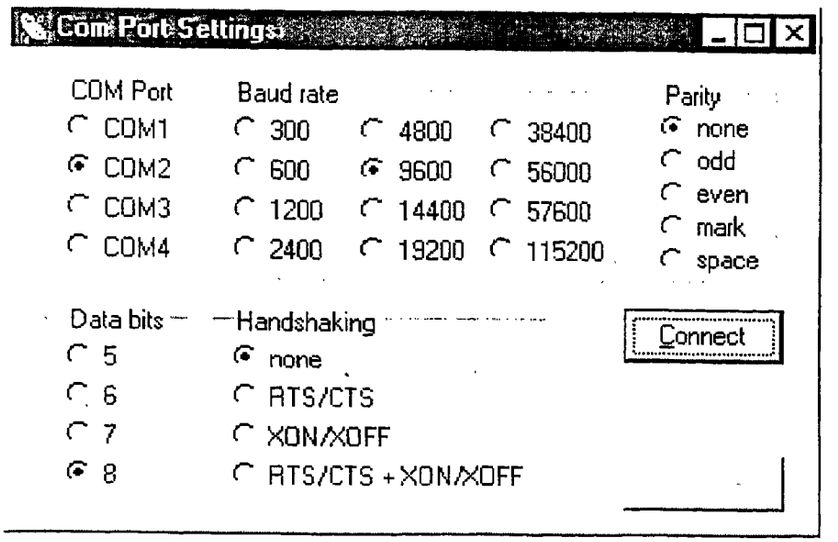


Figure 4.7: Comport dialog

4.5.5 Remote operation

An optical CCD imager forms one of the important back-end focal plane instruments for the 2m telescope at the Indian Astronomical Observatory, Ladakh, designed for remote operation from Bangalore, it is important to support remote operation of the controller. The software should be co-existing with other distributed softwares for the telescope control, dome control etc. We have provided the following features to support the remote operation of the controller.

4.5.5.1 Socket messages

The controller can be operated remotely on a network through socket messaging using TCP/IP protocalls. The data acquisition software is integrated with this option to work under client / server mode. A freeware SOCKETS component (Gary) for Delphi provides an easy to use interface to Winsock functions. The software running on a server connected with the controller can go on to listen mode and a client can get connected to the server. Once a connection is established, commands to the controller can be sent from the client. The

server, in response, sends the status information back to the client. The SOCKETS component properties are used to input IP address, port number, send / receive text, text length etc. The events like OnDataAvailable, OnSessionConnected are useful in coordinating the server/client mode of operation. Messages can also be input in the form of an ASCII file.

4.5.5.2 Virtual network computing (VNC)

The VNC protocol (Tristan et al 1998) allows remote access to the graphical user interfaces. It is based on a concept of remote frame buffer where a server updates the frame buffer on a client viewer. The protocol operates on TCP/IP network. The Windows server (WinVNC) is a server that runs on Windows9x/NT and allows to view the servers desktop from any VNC viewer. WinVNC also allows to log on to server remotely and work on. When a connection is established with the server, the DAS user interface screen is available on the client viewer and the camera can be operated from the client.

4.6 Configuring for the IIA mosaic CCD controller

The CCD acquisition software described above has been interfaced with the mosaic CCD controller described in chapter 3. The Camera: Configure menu opens a configure dialog box as shown in Figure 4.8. The camera can be configured for any one of the 4 CCDs or for mosaic operation. The configuration starts with a downloading of the bootstrap code to the mosaic

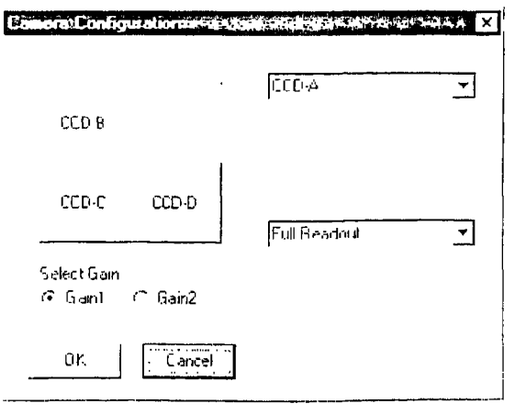


Figure 4.8: Mosaic CCD camera configure dialog

4.6.1 Memory configuration

When a single CCD is selected, a new image of 2K x 2K is created and displayed in the client area of the main window. If a 2x2 mosaic is selected, then a new image of 4Kx4K size is created. The use of multiple CCDs and multiple readouts requires that data be read out in parallel from the CCDs. The raw data is interleaved as it is read and unscrambled before being displayed or stored. Figure 4.9 shows a single CCD with four readout sections, each separated by 512 pixels and a 2x2 mosaic configuration with corresponding readout orientations.

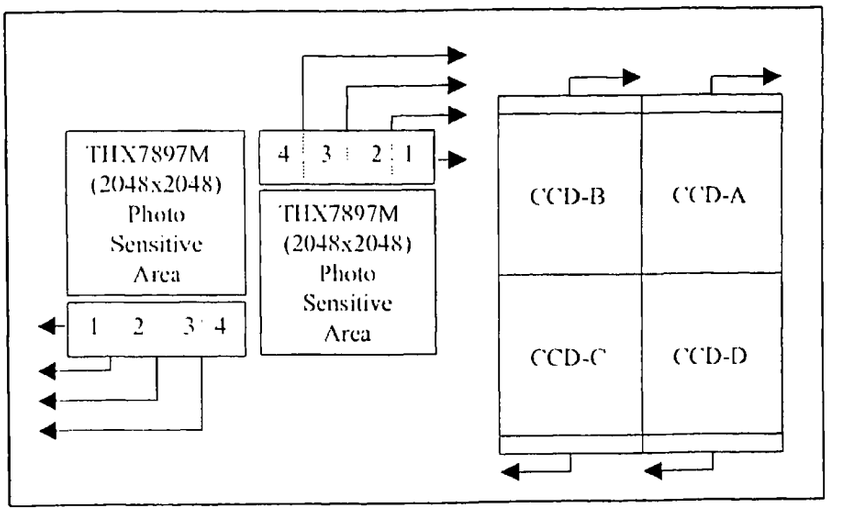


Figure 4.9: Readout orientations in mosaic CCD configuration.

controller and setting of default bias & clock voltages and the ADC offsets. The bias voltages are then enabled. A reset ADC command is then issued to self calibrate the ADC.

4.6.1.1 Handling of memory pointers for single CCD

When a single CCD is selected from the mosaic configuration, the memory pointer has to be configured correctly in order to represent the true orientation of the selected CCD. The core

portion of the data unscrambling is listed in Appendix C and the operation is explained below.

The initial memory pointer, *dataptr*, points to the top-left corner (0,0) for any CCD selected. If the selected CCD is A or B, then the *dataptr* is incremented to point to top-right corner (0,2047) to represent the first readout data point. Since the first 4 data points are separated by 512 pixels, these data are stored in (0,2047), (0,1535), (0,1023) and (0,511) memory locations respectively. The subsequent sets of 4 data points are also stored in the same order but each time decrementing the *dataptr* by one location. After completing the one row of data points (512 x 4), the dataptr is incremented to point to the next row at (1,2047) and the above operation is continued till the entire frame is stored.

If the selected CCD is C or D, then the *dataptr* is incremented to point bottom-left corner (2047,0) to represent the first readout data point. Again, since the first 4 data points are separated by 512 pixels, these data are stored in (2047,0), (2047,512), (2047,1024) and (2047,1536) memory locations respectively. The subsequent sets of 4 data points are also stored in the same order but each time incrementing the *dataptr* by one location. After completing one row of data points (512 x 4), the dataptr is decremented to point to the next row at (2046,0) and the above operation is continued till the entire frame is stored.

4.6.1.2 Handling of memory pointers for the mosaic CCD

If the mosaic CCD configuration is selected, two data pointers, *dataptr1* and *dataptr2* are used to unscramble data points. The dataptr1 points to the top-right corner while the dataptr2 points to bottom-left corner of the mosaic frame. Every serial shift strobes 16 data points, 4 points from each CCD, into the FIFOs in the host interface board. The dataptr1 handles the A and B CCD data (first 8 points) while the dataptr2 handles the C and D CCD data (next 8 points). The dataptr1 and dataptr2 also account for the programmable column gap and row gap in the mosaic configuration.

4.6.2 Configuring bias & clock voltages

While configuring the camera, the default (hard coded in program) bias and clock voltages are programmed in the controller. During development or trouble shooting, it is important to have user access to change these voltages interactively. The SetBiasVoltages / SetClockVoltages dialog boxes shown in Figure 4.10 and Figure 4.11 have been provided to set / modify these voltages as required. The present levels of bias or clock voltages are shown in the respective input boxes. The user can select these values within safe limits (exception occurs if out of range for any CCD. A similar dialog box is provided for setting / changing the ADC offsets.

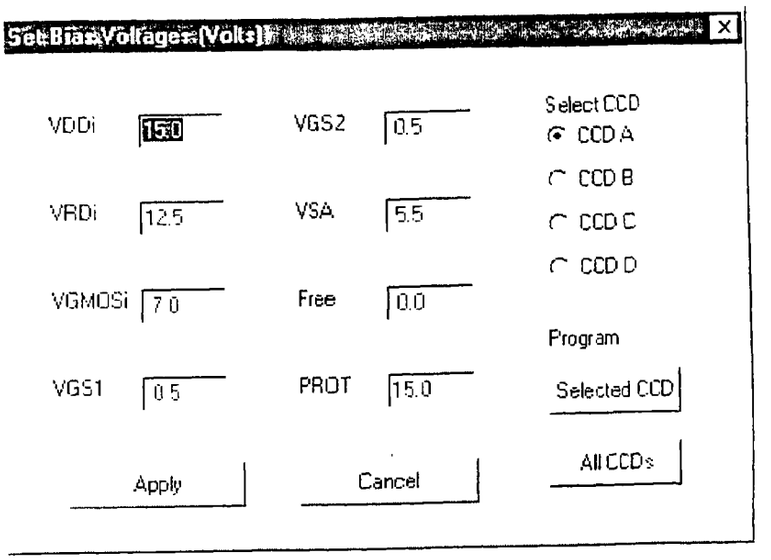


Figure 4.10: Set bias voltages dialog for the mosaic CCD

4.7 Configuring for other controllers

The DAS has been developed to be modular in function. By using SetBias, SetClocks and Camera units any modification needed to suit a particular CCD camera can be set. The DAS has also been configured and successfully tested with a 2Kx4K (ST002AB, dual readout) and a 2Kx2K (SI424, single readout) CCD cameras. The SetBias and SetClocks dialogs have been modified as required for these two camera systems. The Camera unit responsible for

the data transfer from the FIFOs to memory was also suitably modified. As an illustration, the modified dialog box which suits for the ST002AB camera is shown in Figure 4.12.

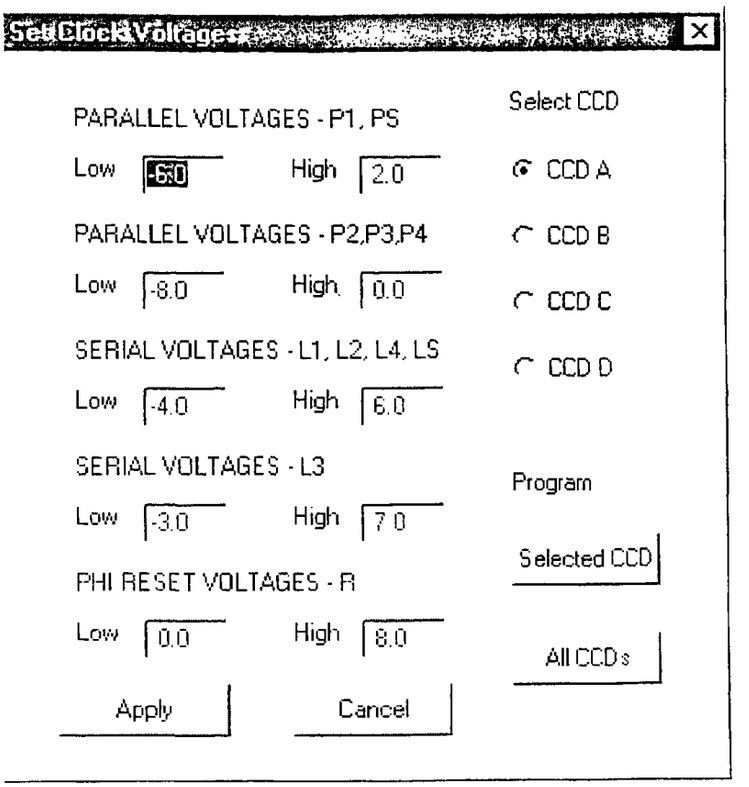


Figure 4.11: Set clock voltages dialog for the mosaic CCD.

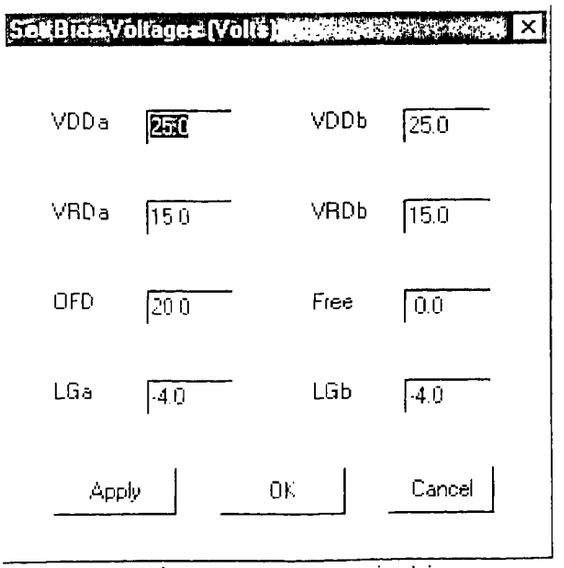


Figure 4.12: Set bias voltages dialog for ST002AB (optical imager)

4.8 Summary

A modular data acquisition and display software has been developed using objects under Delphi. The software has been configured and tested for 2x2 mosaic CCD, and also for other CCDs like ST002AB and SI424. A number of I/O dialogs have been provided for user interaction. Several quick look analysis functions are implemented. A socket message layer has been added to enable remote observations. A filter-wheel utility has also been added to provide filter-wheel selection for the optical imager (ST002AB) CCD camera.

Chapter 5

Calibration and performance of the IIA mosaic CCD camera system

5.1 Introduction

In this chapter, we describe the laboratory setup for measuring linearity, noise/gain and quantum efficiency characteristics of the CCDs along with the performance of the system at telescope. The problem of crosstalk faced in a multi readout CCD is also described and a hardware solution is offered to eliminate the crosstalk between the various readout sections.

5.2 The mosaic CCD camera

5.2.1 Identification of CCDs in the mosaic plane

While procuring the mosaic CCDs, for economy reason, we opted for a wafer-run with M/s Thomson-CSF to produce 3-side buttable CCDs. Out of the 6 CCDs procured from the wafer-run with Thomson-CSF, four were used in a mosaic of 2x2. The devices were selected based on the static tests performed by Thomson-CSF, after UV coating. The static tests included open circuit, short circuit and leakage current on each gate etc. Table 5.1 shows the device identification by manufacturers part numbers and their positions in the mosaic plane. Initially, mechanical samples were used to provide practice in installing the devices onto the mosaic plane before we took up the mounting of the scientific grade devices.

Table 5.1: Part numbers of the CCDs installed in the mosaic plane

Device Part Number (Thomson-CSF)	Location on mosaic plane
408-15-1	CCD-A
408-46-1	CCD-B
408-45-1	CCD-C
408-17-1	CCD-D

5.2.2 Filter / shutter assembly

The sketch of the filter/shutter assembly is shown in Figure 5.1. The filters are broad band UBVRI, procured from Mike Bessel, Mt. Stromlo Observatory, Australia. These are 5mm thick, 127mm round glass filters. The combination of various glasses to produce these filters is shown in Table 5.2. An electromechanical shutter of 100mm clear aperture procured from M/s Prontror (E100) is used to control the exposure times. In order to carry out observations with 1m telescope at VBO, Kavalur, an adopter plate which mates with the position angle device of the telescope was fabricated. The adopter plate is integrated with the filter holder and the electromechanical shutter assembly.

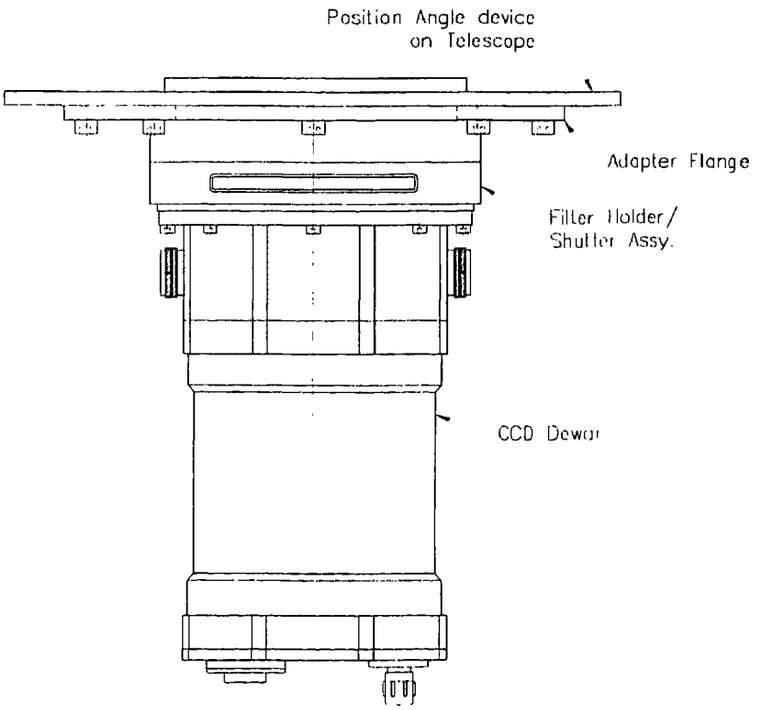


Figure 5.1: Filter / shutter assembly with the mosaic dewar

Table 5.2: Glass combination of filters

Filter	Combination
U	UG1 (1mm) + S8612 (2mm) + WG305 (2mm)
B	BG37(3mm) + BG39 (1mm) + GG395 (1mm)
V	BG40 (3mm) + GG495 (2mm)
R	OG570 (3mm) + KG3 (2mm)
I	RG9 (2mm) + WG305 (3mm)

The laboratory measured transmission for BVRI filters are shown in Figure 5.2

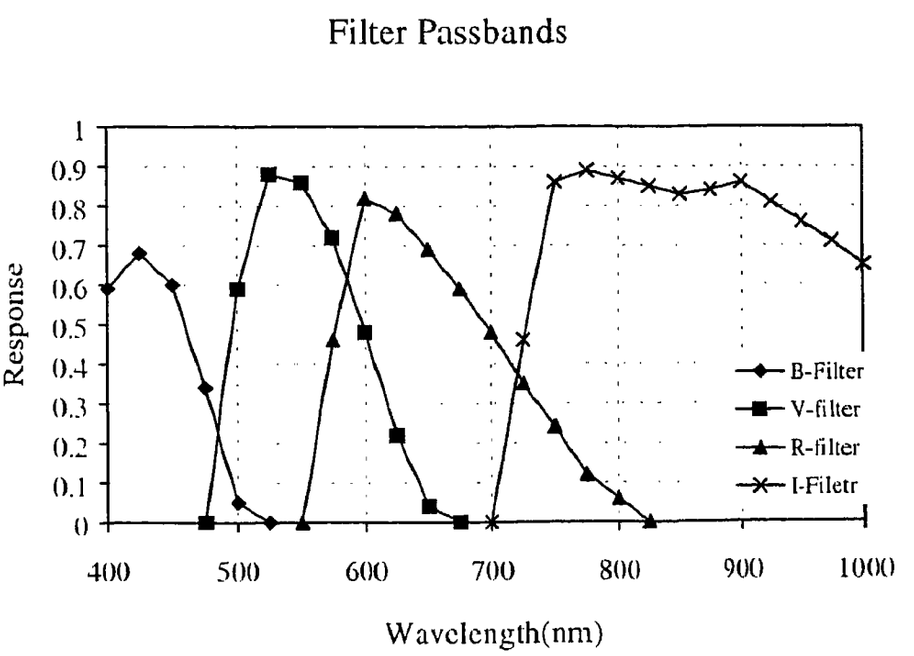


Figure 5.2: BVRI filter passbands

5.3 Laboratory measurements

After an initial satisfactory measurement on bias, dark and light response, a detailed laboratory experiment was setup to characterise the mosaic CCDs, the bias and dark performance, laboratory calibration experiments were conducted to characterize the mosaic CCDs. The following sections describe the experimental setup, the calibration procedure and the results obtained.

5.3.1 Experimental setup

An optical test bench has been setup for carrying out the laboratory tests on the mosaic CCDs. The schematic of the test bench is shown in the Figure 5.3. The main components of the setup comprise of a lamp source, a lamp power supply, a monochromator, an integrating sphere and a light meter.

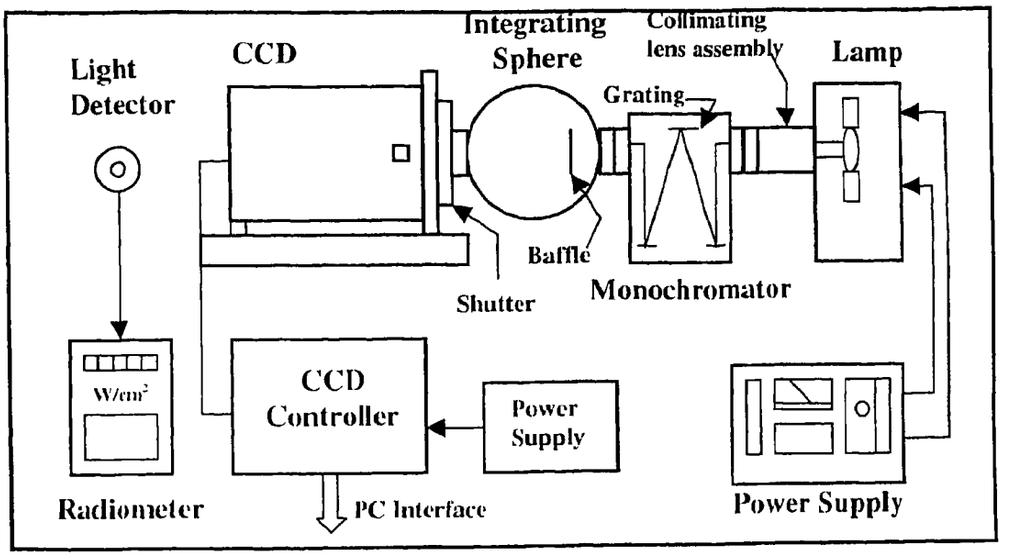


Figure 5.3: CCD calibration experimental setup

A 75W Xenon lamp is mounted in a convection cooled housing with a f/1.5 collimating lens assembly. The collimated beam is 38mm diameter and is focused on the input slit of the monochromator. The lamp is controlled by a constant current supply. The monochromator is Oriel's 77200, that has 0.1nm resolution with narrow slits and accommodates a 1200 lines/mm grating. The usable wavelength range covers from 200nm to 1100nm. A 20cm diameter-integrating sphere from Oriel is used to produce uniform illumination. The sphere has two ports; the input port is 38mm diameter and the exit port is 50mm diameter. The input port of the sphere is aligned to the exit port of the monochromator. A light meter IL1700 supplied by M/s International Light is used to measure the absolute light flux. This light meter uses a calibrated photo diode as detector (silicon SED033) and measures the light intensity directly in watts/sq. cm when programmed with a sensitivity factor at the desired wavelength. The detector response covers from 400nm to 1000nm.

The integrating sphere is attached to a mounting post and fixed to the tabletop. The mosaic CCD dewar is mounted on to a flange which is fixed to the table top. The space between the exit port of the integrating sphere and the dewar is light shielded. The SED033 is used at the same distance where the dewar (CCD) is mounted, in order to measure the absolute light flux.

5.3.2 Noise / gain characterization

A firsthand information on the gain of a CCD system can be determined if the sensitivity of the on-chip output amplifier and the signal processing gain are known. The photon transfer technique gives a more accurate figure for the gain determined through several sets of flats acquired with the system. The following sections describe these methods in detail.

5.3.2.1 Calculated gain of the camera system

The system gain can be calculated based on the output sensitivity of the CCD, pre-amplifier gain, dual slope integration gain of the signal processing chain and the ADC conversion factor using the following relation:

$$\text{System Gain (e}^-\text{/ADU)} = (S_V * A * I_G * ADC_{CONV})^{-1}$$

where S_V is the output sensitivity in $\mu V/e^-$, A is the amplifier gain, I_G is the dual slope integration gain and ADC_{CONV} is in (ADU/μV). For the THX7897 CCDs typical sensitivity is 4.2$\mu V/e^-$. Hence,

$$\text{System gain} = (4.2\mu V/e^- * 1.0 * 5.0 * 1ADU/68.67\mu V)^{-1}$$
$$= 3.27\ e^-/ADU$$

5.3.2.2 Photon transfer curve and measurement of gain

The noise and gain characteristics of the camera can also be found using the photon transfer curve (Janesick et al.1987). The transfer curve is a plot of the variance (square of noise) versus the mean counts. The variance in the signal, σ_e^2, in electrons is given by

$$(\sigma_e)^2 = (\text{Photon noise})^2 + (\text{Read noise})^2$$

Assuming the Poisson statistics, $(\text{Photon noise})^2$ is the signal in electrons which is the intensity in ADU multiplied by the gain (g) in e$^-$/ADU.

$$(g^{*}\sigma_{ADU})^2 = (g * I_{ADU}) + (\text{Read noise})^2$$

$$(\sigma_{ADU})^2 = 1/g *(I_{ADU}) + (\text{Read noise})^2 / g^2$$

So, the inverse of the slope of the plot of $(\sigma_{ADU})^2$ on Y-axis versus (I_{ADU}) on X-axis is the conversion gain in units of e⁻/ADU. The read noise can be obtained by multiplying the σ_{ADU} of a bias frame (zero photon noise) with the system gain.

The input and output slits of the monochromator were adjusted such that a count rate around 1000/sec is obtained. Several pairs of flat images with counts ranging from above the bias level to near saturation were obtained by varying exposure times. The exposure times for pair of flats is kept same. A difference flat from each pair is constructed by subtracting one from another. A small region (40 x 40 pixels) free from pixel defects is selected from the difference image and the variance is computed. The mean levels from the same region in both frames were computed. Similarly, the variance and the mean were obtained for all the pairs of the flat images. The transfer curve was plotted and a straight line was fitted. The gain / noise for all the four readouts in each CCD were thus obtained. The photon transfer plots for the four CCDs are shown in Figure 5.4. Noise rollover is caused by saturation effects as the full-well capacity is reached and the count statistics does not follow Poisson. Table 5.3 presents the gain, noise and full-well capacities obtained from photon transfer plots for the four CCDs in the mosaic.

Table 5.3: Summary of CCD parameters from the measurements (see text)

Parameter	CCD-A	CCD-B	CCD-C	CCD-D
Gain e/ADU	3.92	3.84	3.86	3.87
Noise(e⁻ rms)	19.2	19.2	18.4	18.8
Full-well(ADU)	55,300	60,000	59,000	58,500
Full-well(e⁻)	216,700	230,400	227,700	226,400
Non-linearity (%)	0.36	0.17	0.20	0.1

5.3.3 Quantum efficiency measurements

Quantum efficiency is a measure of the efficiency with which the incident photons are detected. For the wavelengths longer than 300μm, each photon generates one electron-hole pair. The quantum efficiency as a function of the response of the device can be expressed as (Buil Christian, 1991)

$$\text{Quantum efficiency} = (\text{Response}(A/W) * (hc/q\lambda)$$
$$= (N_e q/PS) * (hc/q\lambda)$$
$$= (1.989 * 10^{-25} N_e)/(PS\lambda)$$
$$Qe(\%) = (1.989 * 10^{-23} N_e) / (PS\lambda)$$

where h = the Planck's constant ($6.63 * 10^{-34}$ J.s),
c = Velocity of light ($3 * 10^{8}$ m/s),
q = electron's charge ($1.6 * 10^{-19}$ Coulombs),
N_e = number of collected electrons per pixel per second,
P = Optical power density in W/cm^2,
S = Area of CCD pixel in cm^2
and λ = Wavelength in meters.

The number of electrons collected is obtained from the mean counts (ADU) normalized to 1 second multiplied by the gain (e⁻/ADU). The optical power density is directly obtained from the IL1700 radiometer with a calibrated photodiode. The photodiode is placed at the same distance where the CCD plane was located, and flux measurements were obtained in the range 400 – 1000nm in steps of 25nm. The quantum efficiency is calculated using the above formula at different wavelengths and is presented in Figure 5.5 for the four CCDs.

5.3.4 Linearity tests

The sets of data, which are used to estimate the noise / gain, are also used to plot the linearity curves. A conventional linearity curve – mean versus exposure time was plotted and a quadratic equation fitted. Figure 5.6 shows that the CCDs operate linearly up to their full well saturation. The residuals of the fit show slight non-linearities, the values of which are listed in Table 1 for the four CCDs.

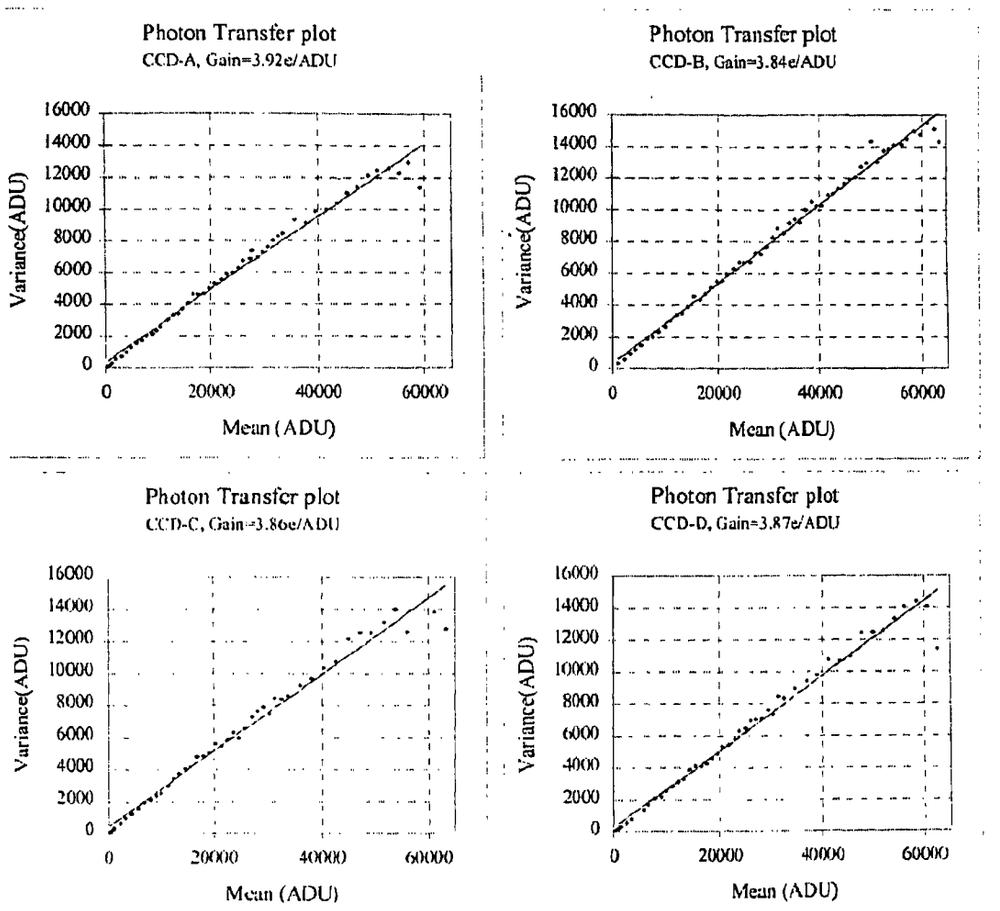


Figure 5.4: Photon transfer plots of individual CCDs in the Mosaic

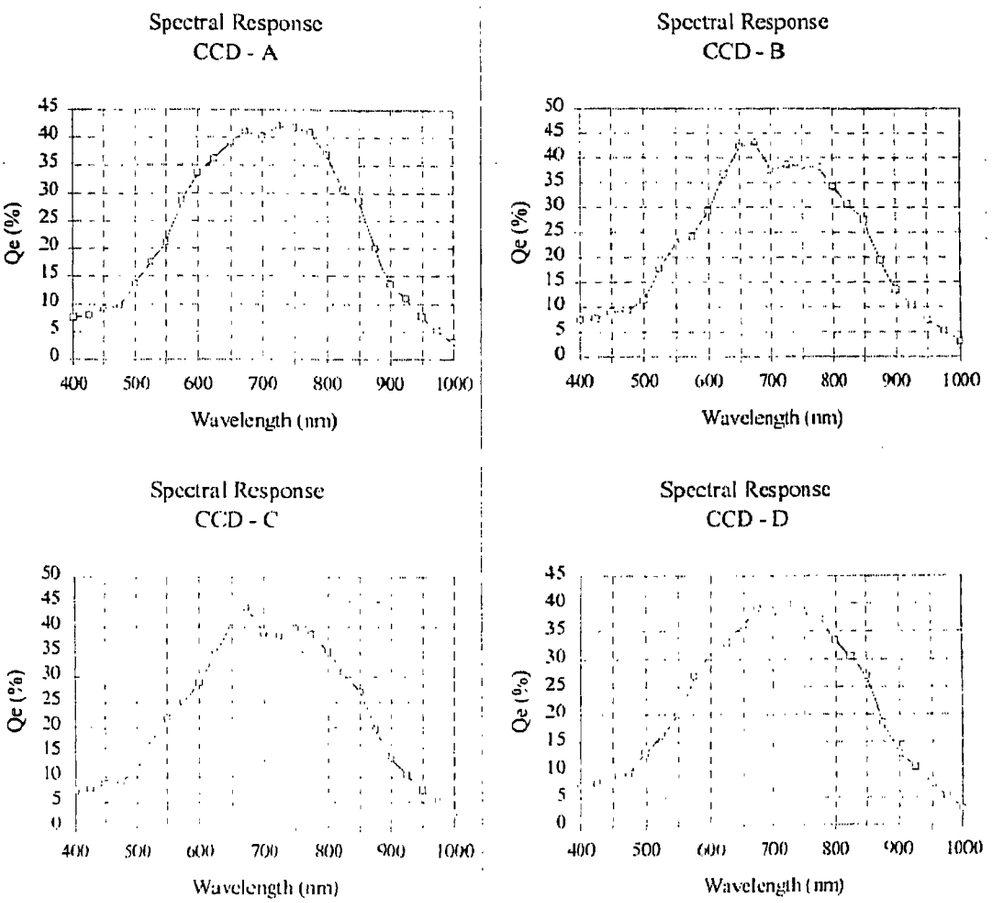


Figure 5.5: The measured Qe for individual CCDs in the Mosaic

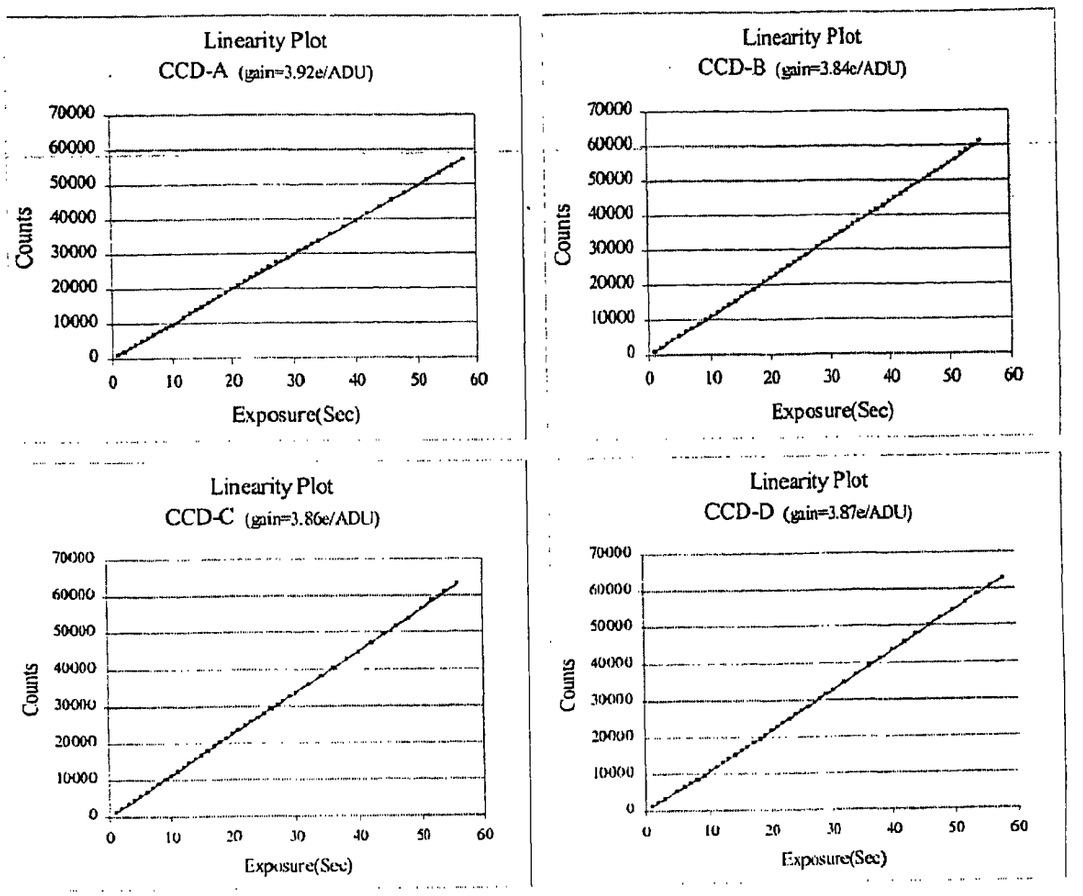


Figure 5.6: Linearity plots for individual CCDs in the Mosaic

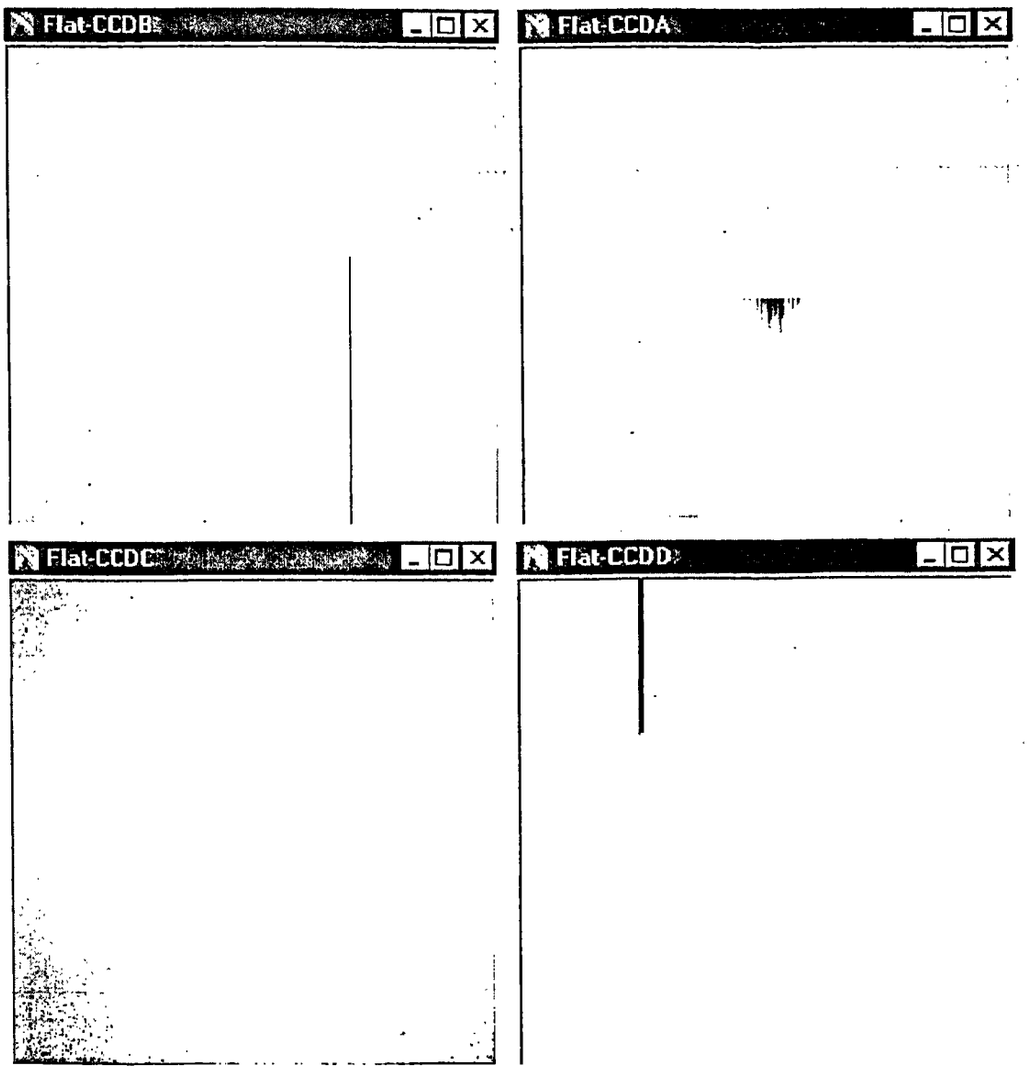


Figure 5.7: Low level flats showing the defects / traps

5.3.5 Traps / defects

Median stack frames obtained from a few low level flats (~ 2000e⁻) is presented in Figure 5.7 for the four CCDs. The column defects (dark) and cluster of defects can be readily seen from these flats. The CCD-A has shown a large trap in the center of imaging area spanning over 1000 columns. The charge transfer subsequent to this trap is affected significantly till end. CCD-B shows 7 column defects (7 columns x 1160 rows) towards the end (opposite to readout register) whose response is only 4% compared with neighboring columns. CCD-C is free from any significant defects. CCD-D also has shown a cluster of column defects (22 columns x 660 rows) responding up to 17%. This cluster defect is also towards the end and hence has no effects on further charge transfer.

5.4 Some problems faced with THX7897 and solutions

5.4.1 Cross-talk in THX7897 devices

The reset FET and the output FET on the readout channel (Figure 5.8) exhibit capacitance from their respective drain to source (C_{DS}), controlling gate to channel etc. The C_{DS} causes signal coupling from source to drain. The gate to channel capacitance causes the feed-through transients on to the signal when the FET is turned on or off. If the CCD has more than one-readout channel, the cross-channel capacitance inter-drain (C_{DD}), inter-source (C_{SS}) can also cause signal coupling between readout channels. The C_{DS} capacitance of each FET on each channel couples some amount of signal onto their respective drains.

A section of an image acquired through one of the THX7898 device is shown in Figure 5.9 where the signal coupling between readout channels can be seen. A signal coupling of about 3 – 4 % in the adjacent readout channels was noticed when all the Reset Drain (VDRi), Output Drain (VDDi) and MOS gate (VGMOSi) supplies (i= 1 to 4) of the readout channels are driven by their respective common voltage sources. If one of the readout channels sees a large signal, the other channels pickup a portion of this signal onto their readout values.

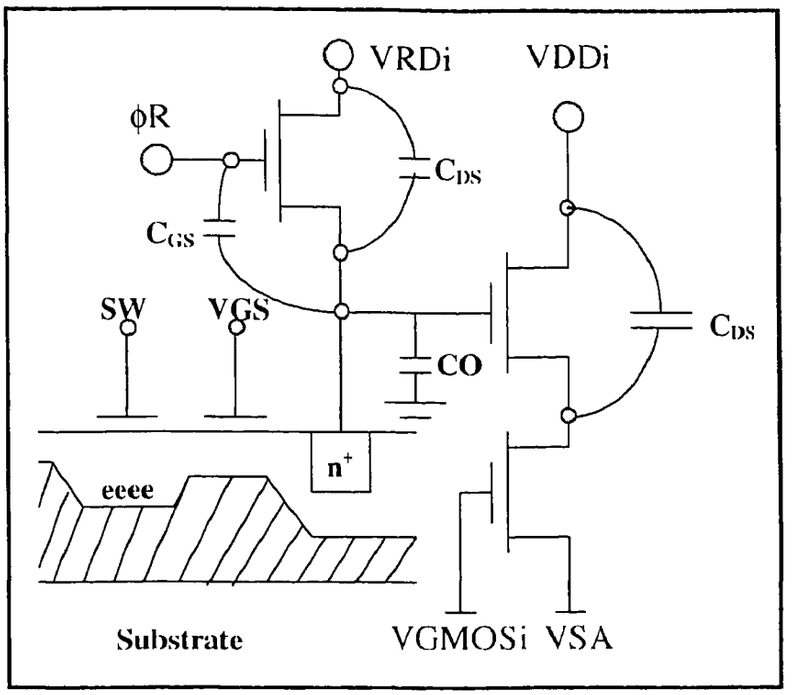


Figure 5.8: Readout stage – signal coupling path

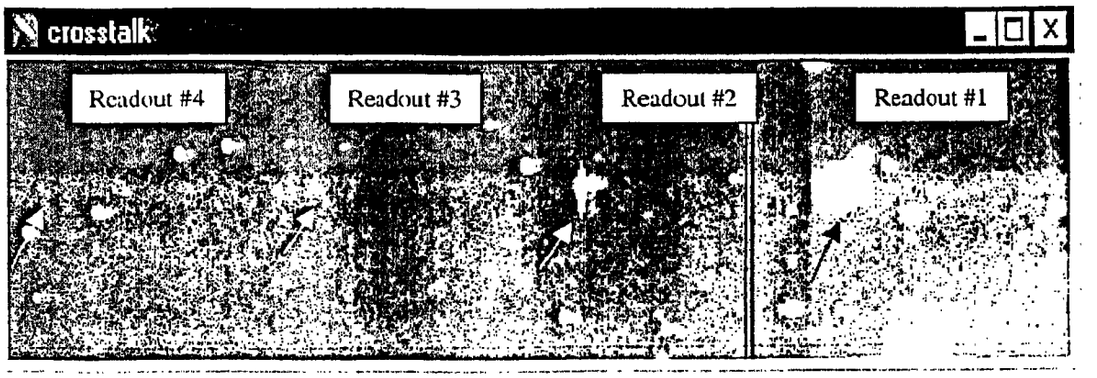


Figure 5.9: Crosstalk between readout channels

One way to eliminate this crosstalk is to provide independent buffers for the bias supplies (VDRi, VDDi and VGMOSi) of the readout channels. Suitable quad voltage buffers were introduced to provide independent bias voltages. This buffering completely eliminated the cross coupling due to the C_{DS} capacitance. The cross coupling due to C_{DD} or C_{SS} is negligible (since they are physically distant from each other) and not noticed in the THX7897 CCDs.

5.4.2 Susceptibility for output failure

A schematic organization of the output amplifier of THX7897 is shown in Figure 5.8. The VGMOS gate voltage sets the drain current through the output amplifier. The data sheets of THX7897 show typical voltage levels for this gate to be in the range 7.5V to 8.0V. During our testing and trial observations two of the devices failed. One output in each of these devices drew excessive current (> 8 mA) from their drain supply. The reason for this failure was investigated and the analysis indicated that the operating voltage for the VGMOS of 7.7V to be rather high and the resulting large drain current could have damaged the output amplifier. Therefore, we have reduced the VGMOS to 7.0V with zener limits set at 7.2V for all CCDs.

Reducing the VGMOS voltage reduces the drain current (I_D), which in turn reduces the transconductance of the output FET. The gain of the output amplifier is given by

$$A = g_m R_L / (1 + g_m R_L)$$

where, g_m is the transconductance of the FET (= dI_D / dV_{GS}) and R_L is the load resistor formed by the current source. The reduction in the transconductance reduces the output amplifier gain, which reduces the system gain also. This is clearly noticed from the calculated and observed system gain parameters as shown in section 3.2. This change endured that no further failures occurred. During long integration times (> 10 min), the VGMOS is set at 5.5V to assure safe operation.

5.5 Performance at the telescope

In order to evaluate the performance of the mosaic CCD at the telescope, it was mounted on the 104-cm Sampurnanand telescope of the State Observatory, Nainital (UPSO) Each pixel of this CCD corresponds to 0.24" at the focal plane of the f/13 telescope beam. An open cluster NGC 6631 was selected for observations. The choice of the cluster was made because the same cluster was earlier observed using the same telescope with another 2K X 2K UPSO CCD system. The UPSO CCD has a pixel size of 24 microns and covers a field of 13' at the focal plane of the telescope.

The cluster was observed in V and I filters on May 9,2001 using the mosaic CCD system. In order to calibrate the observations, standard SA 107 and SA 110 fields from Landolt (1992) were also observed along with a number of bias and twilight flat frames. The data reduction was carried out using IRAF and MIDAS software installed on the

computers of the State Observatory, Nainital. Images were bias subtracted and flat-fielded using standard reduction techniques. As the CCD system is a mosaic of 4 CCDs, each CCD was processed independently. The cluster field is shown in Figure 5.10 and individual CCDs have been marked as A, B, C and D. Further details of the observations and cluster data reductions are presented in Chapter 6.

DAOPHOT software (Stetson, 1987) was used to perform aperture photometry for the standard fields. While observing we placed same set of standard stars on all the four CCDs of the Mosaic. The magnitudes of these standard stars were used to determine transformation coefficients for the four CCDs of the mosaic CCD using following equations:

$$(V - I) = p_1*(v - i)_0 + q_1$$

$$V = v_0 + p_2*(V - I)_0 + q_2$$

where **V, I** are the standard values while v_0, i_0 are the extinction corrected CCD instrumental aperture magnitudes, p_1, p_2 are the transformation coefficients and q_1, q_2 are zero-points. The values of these constants for all 4 CCD chips are listed in Table 5.4. The values of transformation coefficients indicate that the characteristics of all the four CCDs of the mosaic are almost identical and the filter combination closely reproduces the standard photometric system.

Table 5.4: Transformation coefficients of the mosaic CCDs:

Coeff.	CCD-A	CCD-B	CCD-C	CCD-D
p_1	1.078	1.081	1.087	1.077
p_2	0.125	0.113	0.118	0.116

As there are physical gaps in the mosaic CCD system, it is necessary to precisely evaluate the dimensions of these gaps. This information is necessary to bring the positions of stars in different CCDs to a common reference. We have compared the position of stars of the cluster observed through UPSO CCD with the positions observed in the mosaic CCD to evaluate these inter gaps. The values of these gaps have been shown in Figure 5.10. Though the physical gaps are typically 0.8mm, since each CCD has dead zones (no CCD pixels) of 0.2mm on one side and 0.4mm on other two sides, the total missing gap between two CCDs is 1.2mm in X-direction (parallel to readout registers) and 1.6mm in Y-direction.

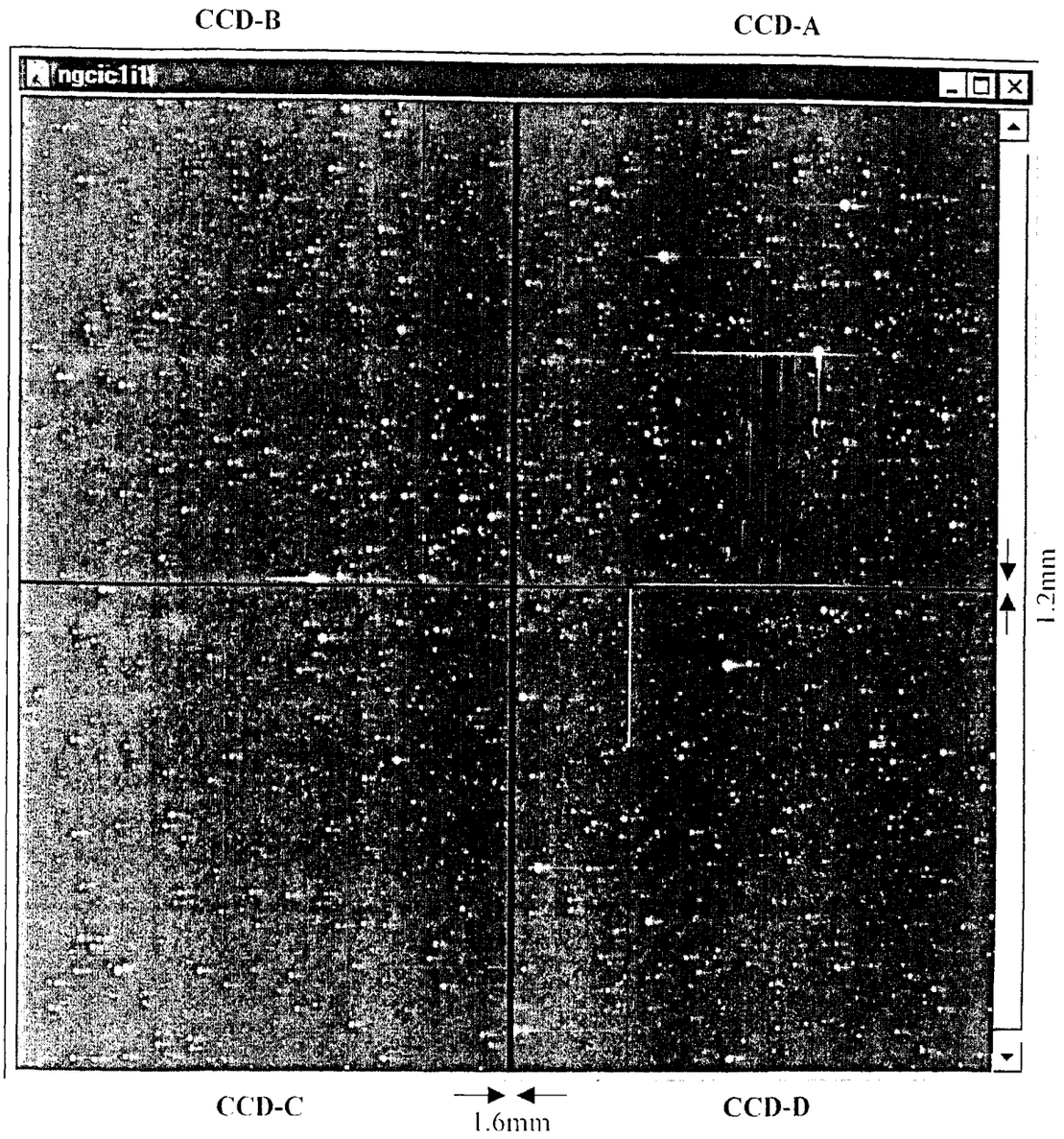


Figure 5.10: NGC6631 Cluster

Table 5.5 Statistical results of the photometric comparison of the present **VI** CCD data with those obtained using the 2K X 2K CCD camera of the State Observatory, Nainital. The difference (Δ) is in the sense UPSO minus present data. The mean and standard deviation (σ) are based on **N** stars. A few points discrepant by more than 3σ have been excluded from the analysis.

V Range	$\Delta V \pm \sigma$	N	$\Delta(V-I) \pm \sigma$	N
10-14	0.01±0.03	64	-0.02±0.04	63
14-16	0.00±0.03	361	~0.00±0.05	352
16-17	-0.02±0.04	420	~0.00±0.07	412
17-18	0.00±0.07	783	~0.02±0.09	784
18-19	0.04±0.10	1380	~0.06±0.14	1382
19-20	0.06±0.11	811	~0.08±0.15	813

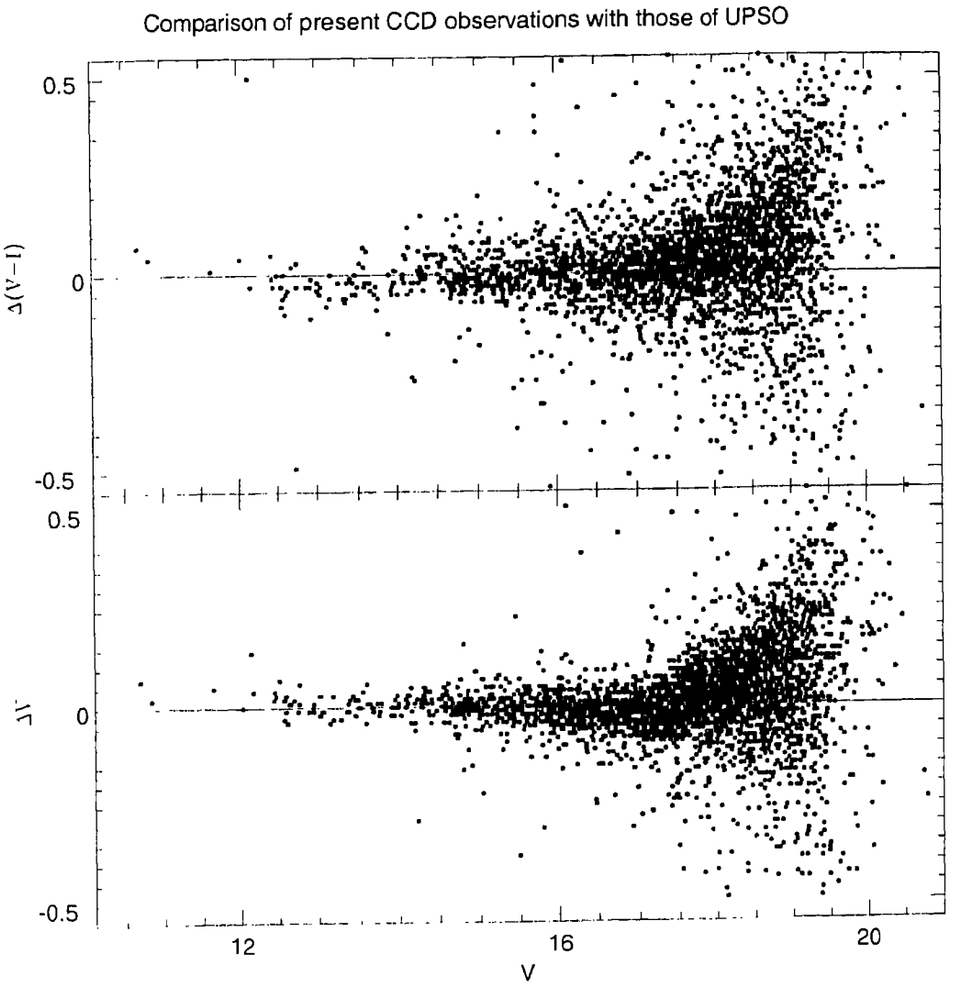


Figure 5.11 Comparison of present CCD observations with those of UPSO CCD

We have also compared the magnitudes and colours obtained from the mosaic CCD and the UPSO CCD for the cluster. The differences in V and (V-I) magnitudes are plotted in Figure 5.11 as a function of V magnitude and the statistical results are listed in Table 5.5. These show that the distribution of the photometric differences seems fairly random except for a few outliers, which appear to be mostly stars that were treated as single in one CCD study and as blended doubles in other. As expected, the scatter increases with decreasing brightness and becomes more than ~0.1 mag for stars fainter than **V = 18** mag. Considering these and the uncertainties present in photometric measurements, we conclude that the performance of the 4K X 4K mosaic CCD is satisfactory at the telescope.

5.6 Conclusions

The laboratory experimental setup and characterization / calibration procedures are described. The 4Kx4K mosaic CCD camera system developed at IIA has been characterized. All four CCDs in the mosaic match similar characteristics. The system gain and noise figures for the four CCDs are close to each other. The quantum efficiency measurements are more or less same for these four CCDs and closely agree with the typical THX7897 Qe curve. The crosstalk between the different readout sections could be eliminated by suitable buffering of certain bias supplies. The performance of the mosaic CCD, is evaluated by observing an open cluster NGC6631 and comparing the results obtained from previous observations of the same cluster by the UPSO 2Kx2K CCD system. The results indicate a satisfactory performance at the telescope.

Chapter 6

Study of the star cluster - NGC 6631

6. 1 Introduction

The Galactic star clusters are valuable tools for the studies of a number of present day astrophysical problems. For such studies, a knowledge of cluster parameters and stellar content are mandatory and they are lacking for more than 60 % of the star clusters of our Galaxy. In an attempt to provide such parameters, number of open star clusters from both northern and southern hemisphere of our Galaxy were observed and the cluster parameters derived from their deep colour magnitude diagrams (CMDs) were given by Sagar & Cannon (1994), Sagar Griffiths (1999), Subramaniam & Sagar (1999) and Sagar, Munari & de Boer (2001). In this chapter, we present a detailed *VI* photometric study of the NGC 6631 observed with the mosaic CCD camera system described in chapter 5.

The neglected open star cluster NGC 6631 (≡C1824-120 ≡ OCL 59 ≡ Lund 833) with l = 19.°47 and b = -0.°19 is located in the direction of Galactic center. Ruprecht (1966) classified the cluster as **II**2m while Lyngå (1987) call it as **II**1m. So far, no photometric study has been presented for the cluster. In the compilation of cluster parameters by Alter et al. (1971), the values of angular diameter range from 4 to 16 arcmin while those of distance varies from 880 to 5000 pc, indicating clearly a large uncertainties in the parameters of NGC 6631. A deep and accurate photometric observations are therefore essential for the cluster and the same has been provided here. The details of the telescope and CCD camera used in the observations are given in the next section along with the

procedures of photometric data reduction and calibration. The morphology of the CMD and parameters of the cluster are presented in the remaining part of the chapter.

6.2 Observations and data reductions

The *VI* CCD photometric observations were obtained during May 8 to 10, 2001. For this the mosaic CCD camera (Naidu et al 2001), the details of which are described in chapters 2 - 5 was mounted on the 104-cm Sampurnanand telescope of the State Observatory, Nainital. Each pixel of this CCD corresponds to 0."24 at the Cassegrain focus of the f/13 telescope. The NGC 6631 was observed in Johnson *V* and Cousins *I* passbands. The area covered is about 16' x 16' (see Figure 6.1). In order to calibrate the cluster observations, two standard (SA 107 and SA 110) fields from Landolt (1992) were also observed. The log of observations is given in Table 6.1. A number of bias and twilight flat frames were also taken to calibrate the images. The data reduction was carried out using IRAF and MIDAS softwares installed on the computers of the State Observatory, Nainital. Images were bias subtracted and flat-fielded using standard reduction techniques. As the CCD system is a mosaic of 4 CCDs, each CCD was processed independently. The gaps of about 25 arcsec width due to mosaic of CCDs can be clearly noticed in Figure 6.1.

In order to improve the signal to noise ratio of the photometric measurements, the images of the cluster are aligned and co-added in each filter and also linearly re-binned with a factor of 2. The full width at half maximum of such stellar images is about 4 pixels. Although the observed cluster NGC 6631 region is not exceptionally crowded, the magnitude estimation of star has been carried out using DAOPHOT profile-fitting software, as described by Stetson (1987, 1992), so that it can be determined reliably to faint levels. The stellar PSF used by DAOPHOT is evaluated from the sum of several uncontaminated stars present in each frame. The DAOPHOT photometric errors and image parameters χ and sharpness are used to reject poor measurements. About few per cent of measured stars are rejected in this process.

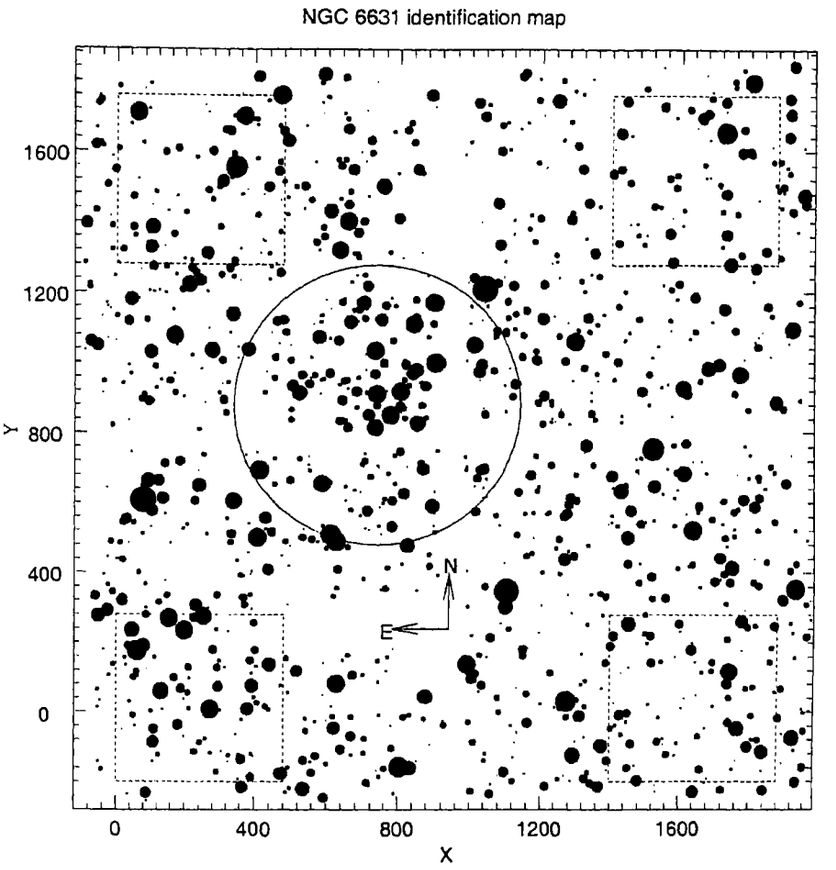


Figure 6.1: Identification map for the observed region around NGC 6631. The (X, Y) coordinates are in pixel units and pixel corresponds to 0."48 on the sky. North and East directions are marked. The size of star denotes the brightness, smallest size being for V = 17 mag star. Circle denotes the cluster region while dotted squares show the regions used for the determination of field star contamination.

Table 6.1: Log of CCD photometric observations of cluster NGC 6631 and Landolt (1992) SA 107 and SA 110 standard fields.

Date	Field	Filter	Exposure (Sec)
9/10 May 2001	SA 107	I	100x5
9/10 May 2001	SA 107	V	200x6
9/10 May 2001	NGC 6631	I	300x4
9/10 May 2001	NGC 6631	V	300x8
10/11 may 2001	SA 110	I	100x12
10/11 may 2001	SA 110	V	300x12

The transformation equations used to transfer instrumental magnitudes to the standard photometric system are:

$$(V - I) = p_1(v - i)_0 + q_1 \text{ and}$$

$$V = v_0 + p_2(V - I) + q_2;$$

where V, I are standard magnitudes taken from Landolt (1992) and v_0, i_0 are atmospheric extinction corrected instrumental CCD aperture magnitudes. p_i and q_i are the colour coefficients and zero-points respectively. For the standard fields SA 107 and SA 110 aperture photometry was performed. While observing, we placed same set of SA 110 standard stars on all the four CCDs of the Mosaic. They cover a range in brightness ($11.7 < V < 14.7$) as well as in colour ($0.65 < (V-I) < 2.6$). The magnitudes of the 7 standard stars are used to determine p_i for the four chips of the mosaic CCD and the values were listed chapter 5. These transformation coefficients indicate that the characteristics of all the four CCDs of the mosaic are almost identical and the filter combination closely reproduces the standard photometric system.

Extinction coefficients and zero points were determined using the stars in the standard field of SA 107 as these were observed on the same night on which the cluster NGC 6631 was observed. The magnitudes of stars in the cluster field were then standardised using the slopes (p_i) obtained from SA 110 and zero points (q_i) from SA 107.

The (X, Y) pixel coordinates, V and (V-I) magnitudes of the sample stars observed in NGC 6631 are listed in Table 6.2 along with DAOPHOT errors. The format of the Table 6.2 is presented here while the entire data is available only in electronic form at the open cluster database website at **http://obswww.unige.ch/webda/.** It can also be obtained from the authors. Stars are numbered in the ascending order of X. There are 5533 stars observed in the region imaged by us. They are fainter than $V = 12$ mag. In Figure 6.2, we plot the magnitude errors as a function of the brightness for both V and I magnitudes. The DAOPHOT errors are ~0.15 mag at $V = 20$ mag. We have therefore not considered stars fainter than this as the measurements are unreliable.

6.2.1 CMDs based on present observations

The apparent V, (V-I) diagram generated from the present data are displayed in Figure 6.3. The deep CMD extends down to $V = 20$ mag. A broad main-sequence (MS) with

some red gaints belonging to both cluster and field populations is visible in the CMD. It is difficult to separate field stars from the cluster members only on the basis of their closeness to the main populated area of the CMD because field stars at cluster distance and reddening will also occupy this area. However, the possibility of cluster membership is small for the stars located well away from the eye defined blue and red envelopes of the MS (see Figure 6.3). To know the actual number of cluster members from the remaining stars, their precise proper motion and/or radial velocity measurements are required. In the absence of such data, we used the statistical criteria of the cluster membership in the next section.

Table 6.2: Sample of *VI* photometric data of the stars around the NGC 6631 cluster region. X, Y are the CCD pixel coordinates shown in Figure 6.1. σ_V and σ_I are the DAOPHOT errors in the *V* and *I* bands respectively.

Star	X (pixel)	Y (pixel)	*V* (mag)	(*V-I*) (mag)	σ_V (mag)	σ_I (mag)
1	-124.94	1165.81	20.41	2.81	0.37	0.05
2	-102.05	1284.94	18.63	2.43	0.08	0.01
203	-9.12	416.96	18.58	1.36	0.05	0.03
204	-8.88	-225.68	17.00	1.54	0.01	0.01
1405	393.18	1560.59	18.22	1.40	0.05	0.02
1406	393.54	1742.67	18.89	2.04	0.07	0.04

6.3 Radial stellar surface density and field star contamination

The radial variation of stellar surface density derived from the present data can be used to verify clustering, determine cluster radius and also to estimate the extent of field star contamination in the cluster region. For this, the cluster center is determined first. Its (*X*, *Y*) pixel coordinates (745,880) are derived iteratively by calculating average *X* and *Y* positions of the stars within 200 pixels average from an eye estimated center, until the values coverage. An error of few tens of pixels is expected in locating the cluster center. For determining the radial surface density of stars, the imaged area has been divided into a number of concentric circles with respect to cluster center, in such a way that each annulus region contains statistically significant number (> 40) of stars. The number density of stars in the *i*th annulus is given as $\rho_i = N_i / A_i$; where N_i is the number of stars in the area A_i of *i*th annulus. The radial density profile thus obtained is plotted in Figure

6.4. The presence of clear radius density variation in the figure confirms the existence of clustering in NGC 6631.

6.3.1 Cluster radius

As the cluster lies in the galactic plane in the direction of Galactic center (l = 19.5°, b=-0.2°) the field star density is high with value about 85 star/arcmin2. The peak density value in Figure 6.4 is about 150 star/arcmin^2. The radius at which the value of ρ becomes approximately equal to the field star density has been considered cluster radius and it turns out to be ~400 pixel ≡ 3.2 arcmin. The accuracy of the determination is ±0.3 arcmin. The present radius estimate agrees well with the value of 3 arcmin given by Lyngå (1987).

6.3.2 Field star contamination

The mosaic CCD covers a field of ~ 16' square. As the cluster diameter is only 6.'4, the remaining region can be used to study the distribution of field stars around the cluster. For this, we use four square regions located in the four corners of the imaged field as shown in Figure 6.1. Each region covers an area of 480 pixel (≡ 3.'8) square. The central pixel coordinates of the field regions 1, 2, 3 and 4 are (240, 1520), (240, 40), (1640, 1520) and (1640, 40) respectively. The field regions thus lie at 2.1 to 3.1 cluster radius with an average value of 2.6 from the cluster center. The frequency distribution of stars in different parts of the V, $(V\text{-}I)$ diagram of the field regions is listed in Table 6.3. To derive it, the diagram is divided into 8 magnitude bins from V = 12 to 20 and three colour bins with $(V\text{-}I) < 1.0$, $(V\text{-}I) = 1.0$ to 2.0 and $(V\text{-}I) > 2.0$. Table 3 indicates that within Poisson errors, the frequency distribution of stars in different part of the V, $(V\text{-}I)$ diagrams of all the 4 field regions agree with each other. From this, we conclude that the distribution of field stars around cluster region can be assumed uniform and the field stars contamination in the V, $(V\text{-}I)$ diagram of cluster region can be estimated statistically. The frequency distributions shown in Table 6.3 indicate that the present photometric observations appear to be complete only up to $V = 19$ mag.

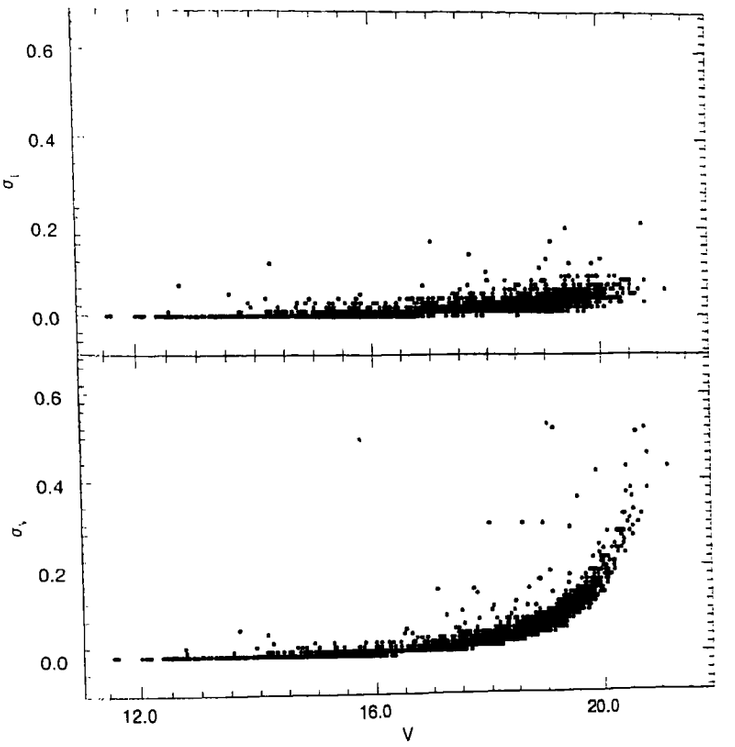


Figure 6.2: The DAOPHOT errors in V and I as function of V for stars of the cluster region.

Table 6.3: Frequency distribution of stars in the V, (V-I) diagrams of the four field regions. The colour bins C1, C2 and C3 have (V-I) values <1.0, 1.0 to 2.0 > 2.0 respectively.

	(V-I) Colour Bins for											
V range (mag)	Field 1			Field 2			Field 3			Field 4		
	C1	C2	C3	C1	C2	C3	C1	C2	C4	C1	C2	C3
12 to 13	4	0	0	2	0	2	0	2	0	2	0	0
13 to 14	6	0	0	3	0	3	2	0	0	7	0	0
14 to 15	8	5	0	6	11	2	11	17	2	14	13	0
15 to 16	23	28	0	20	25	2	11	25	4	22	18	0
16 to 17	7	65	2	9	58	8	0	61	0	11	84	0
17 to 18	4	142	13	2	114	11	0	106	7	5	132	4
18 to 19	0	202	20	2	149	25	2	171	2	0	175	4
19 to 20	2	60	19	0	57	22	2	64	21	2	65	7

In order to define morphological features of the cluster in the CMD accurately and also for reliable estimation of the colour excess, distance modulus and age of the cluster, we have included only those stars in our further analysis which are lying within a cluster

radius from the cluster center. By doing this, we have enhanced the ratio of cluster to field stars in the sample which makes the cluster sequence better defined in the *V*, (*V-I*) diagram shown in Figure 6.5. To quantify the field stars still present in the diagram, the boundaries of the MS (see Figure 6.3) has been superimposed in the CMD of the cluster and field regions. Frequency distribution of the stars in different parts of their *V*, (*V-I*) diagrams normalized for the difference in their areas is listed in Table 6.4. For this, the *V*, (*V-I*) diagram is divided into 7 magnitude bins from *V* =12 to 19 and three colour bins called *blueward*, *near* and *redward* of MS. We find that the number of cluster MS stars is generally more than that in the field region and that the differences are mostly statistically significant, while the number of stars, which are blueward and redward of cluster MS, of the two regions are generally similar in the statistical sense. The table indicates that the degree of field-star contamination in the cluster MS is increasing with faintness, as expected. Table 6.4 also indicates that some of the red gaints brighter than *V* = 13.5 mag belong to the NGC 6631. The cluster parameters are derived using stars of the cluster region assuming that field star contamination may not change the results derived below significantly.

Table 6.4: Frequency distributions of stars in the V, (V-I) diagrams of the cluster and field regions are presented. The number of stars in the field region is normalised to the cluster area. N_{BC}, N_{MC} and N_{RC} denote the number of stars in the cluster region located blueward, near and redward of MS respectively. The corresponding numbers for the field region are N_{BF}, N_{MF} and N_{RF} respectively. N_C ($\equiv N_{MC} - N_{MF}$) denotes the number of MS cluster members.

Range in V mag	N_{BC}	N_{BF}	N_{MC}	N_{MF}	N_{RC}	N_{RF}	N_C
12.0 – 13.0	1	1	7	2	4	2	5
13.0 – 14.0	1	1	6	4	4	1	2
14.0 – 15.0	4	1	20	8	8	13	12
15.0 – 16.0	1	0	34	23	26	22	11
16.0 – 17.0	8	2	52	40	30	32	12
17.0 – 18.0	9	12	108	75	51	49	33
18.0 – 19.0	30	24	127	115	43	47	12

6.4 Determination of cluster parameters

The MS stars along with all the stars brighter than *V* = 13.7 mag of the cluster region (radius ≤ 400 pixel) are used to determine cluster parameters. In Figure 6.5, we plot the *V*, (*V-I*) diagram for these stars. A broad but well-defined cluster MS in the magnitude

range of $19 \leq V \leq 12$ and the effects of stellar evolution in the brighter stars are clearly visible. Broadening of the MS appears to be increasing with the faintness of the star. In order to see whether part of the MS broadening is due to non-uniform extinction across the face of cluster or not, we divided the cluster region into four equal regions and estimated the scatter in the V, $(V\text{-}I)$ diagram of each region with respect to the isochrone adopted below for age estimate. It is found that scatter is almost similar in the CM diagrams of different regions of the cluster. This indicates that the inclusion of field stars, the presence of binaries, intrinsic variables and peculiar stars etc in the sample are responsible for intrinsic width of the MS though it is not possible from this study to assess their relative contributions to such a spread. As most of the factors responsible for the colour spread in the MS will redden the stars, we have used the blue envelope of the MS in CM diagram for the estimation of cluster parameters.

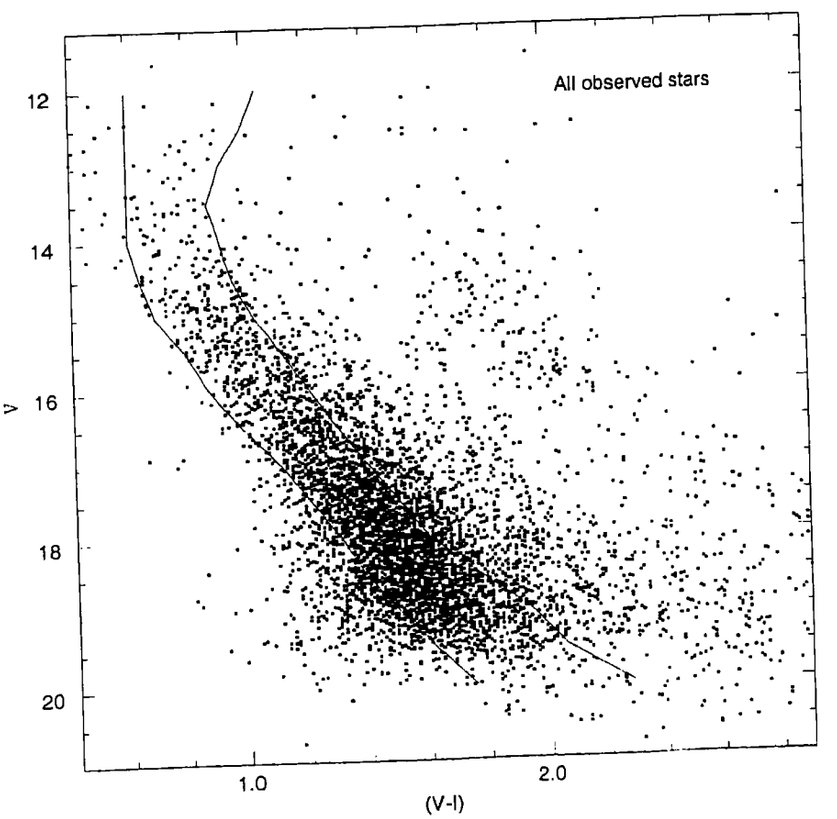


Figure 6.3: The V, $(V\text{-}I)$ diagram for all the measured stars around NGC 6631 with the envolopes delimiting MS stars.

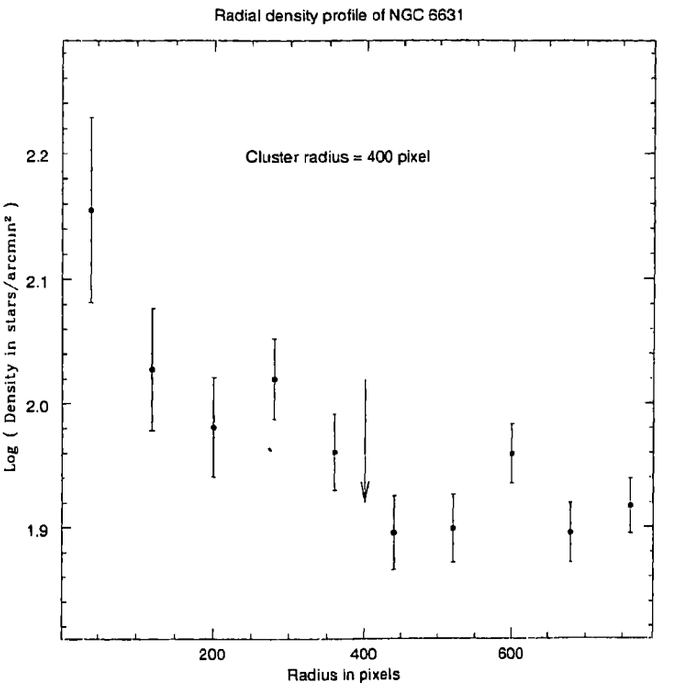


Figure 6.4: Plot of the radial stellar density profile determined from our data against radius in pixels with respect to the cluster center (Xc = 745, Yc = 880). Arrow denotes the radius where the stellar density seems to merge with the field-star density and it corresponds to 3.2 arcmin.

Bertelli et al. (1994) theoretical stellar evolutionary isochrones are used to estimate the parameters of the cluster. As the metallicity is not known spectroscopically for the cluster, we assumed that it may have solar or higher metallicity, as the cluster is located in the direction of Galactic center. We have fitted the isochrones by eye to the blue part of the long MS, turn-off point and also to a few possible red giants in Figure 6.5. We find that the ischrone corresponding to metal-rich model (Y=0.352, Z=0.05) for an age of 400 Myrs (log (t) = 8.6) fit the data reasonably well. In this process, the colour spread expected from the observational error as well as from the binarity and peculiarities has been taken into account. In order to define upper limit of the effects of binarity in Figure 6.5, the isochrones which are derived from theoretical stellar evolutionary models or single stars have been brightened by 0.75 mag keeping the colour same. The isochrones fitted in this way explains the presence of stars around the MS turn-off point. This also indicates that some fraction of cluster members seems to be in the form of binaries. In stars fainter than V = 16 mag, strong field star contamination in the cluster MS, as also

quantified in Table 6.4, can be clearly noticed. The values of other cluster parameters derived in this way are $E(V\text{-}I) = 0.60\pm0.05$ mag *and* $(V\text{-}M_V) = 13.5\pm0.3$ mag. Adopting a normal value of total to selective absorption ratio, R ($\equiv A_V/E(V\text{-}I)$) = 2.3, yields a true distance modulus of 12.1±0.4 mag corresponding to a distance of 2.6±0.5 kpc for the cluster. We expect an uncertainty of about 100 Myr in the age estimates. The errors are estimated from the errors in R, photometry, and the error in the fitting of the isochrones.

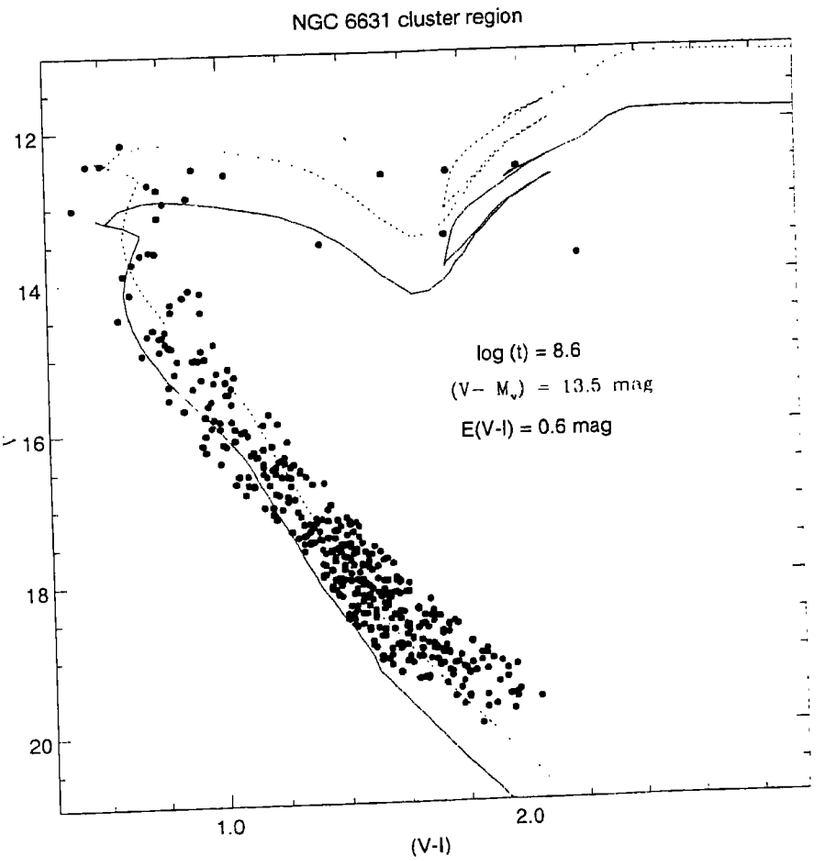


Figure 6.5: Theoritical isochrones given by Bertelli et al. (1994) for metallicity Z = 0.05 fitted to the MS, turn-off point and the red gaints of the NGC 6631 in V, $(V\text{-}I)$ diagram for the marked values of distance modulus., colour excess and log of age. The dotted curve shows the extent that binaries of the same mass can brighten the isochrones. All stars brighter than $V = 13.7$ mag and the MS stars of the cluster region have been plotted here.

6.5 Mass function of the NGC 6631

The mass function (MF) of the cluster NGC 6631 is determined from the MS luminosity function of both cluster and field regions listed in Table 6.4. The cluster MS luminosity function corrected for field star contamination ($N_C = N_{MC} - N_{MF}$) is given in Table 6.4. The transformation of V to M_V and finally into mass (M) is done using cluster parameters derived above and the mass-luminosity relation for the isochrone of cluster age and metallicity given by Bertelli et al. (1994). The MF derived in this way is plotted in Figure 6.6. The stellar MF in

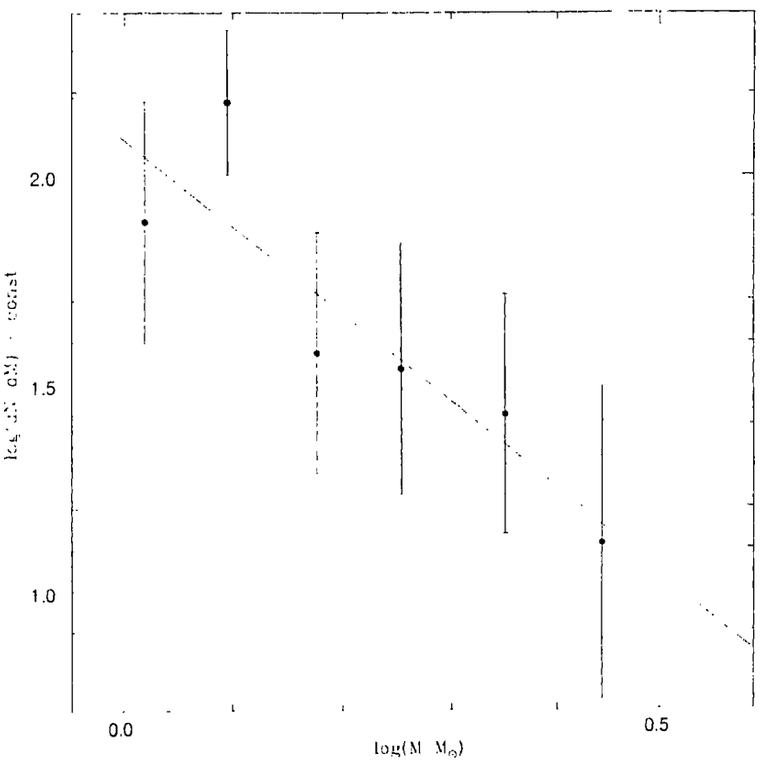


Figure 6.6: A plot of the NGC 6631 mass function. The bars represent 1/N poisson errors. Solid line of slope 2.1 denotes the least squares linear fit to the data points.

a limited mass interval is generally expressed as a power law $dN \propto M^{-\alpha}dM$, where dN is the number of stars in the mass interval dM and α is the slope of the MF. We therefore fit least squares linear relation to the data points which yields a value of 2.1±0.5 for the MF slope. As the Salpeter (1955) value of MF slope on this scale is 2.35, the cluster MF slope agrees with it.

6.6 Conclusions

For the first time, the V and I CCD photometry down to V = 20 mag is presented for about 5,500 stars in the wide region around open cluster NGC 6631. The present work leads to the following conclusions: -

The cluster parameters derived by visual fitting of the theoretical stellar isochrones to the V, $(V\text{-}I)$ diagram over a broad range of V magnitude (~ 6) and also to the turn-off region are $E(V\text{-}I)$ = 0.60±0.05 mag, apparent distance modulus = 13.5±0.3 mag, age = 400±100 Myr and metallicity higher than solar.

The radial distribution of stellar surface density clearly showsclustering in NGC 6631. This also indicates that angular radius of the cluster is 3.2±0.3 arcmin.

The slope 2.1±0.5 of the cluster MF is similar to that of Salpeter (1955) MF.

The cluster has well defined MS. Effects of stellar evolution are clearly visible at the brighter end of the CMD. In absence of kinematical data, it is difficult to separate cluster members from the field stars unambiguously only on the basis of present observations.

The broad main sequence has been observed in the CM diagram of the cluster. The most probable sources of MS broadening are observational errors, the presence of field stars, binaries, variables and peculiar stars in the sample. Fitting of the isochrones in the CMD indicates that some fraction of the cluster members are binaries.

Chapter 7

Conclusion and some suggestions on improvement

7.1. What has been achieved?

A camera system suitable for any/mosaic CCDs has been built during this thesis work. The generality of the hardware was made possible by incorporating a Digital Signal Processor into the control electronics. The DSP's program is downloaded from a PC permitting complete flexibility in timing and sequencing of the detector and its associated electronics. As part of the camera system, the following hardware and software were implemented and tested.

A modular cryostat has been successfully fabricated incorporating suitable mountings for the mosaic (THX 7897M) as well as single CCDs like SITe ST002AB & SI424. The cryostat met the two important requirements of (i) a Liquid Nitrogen holding time > 24 hours and (ii) a satisfactory vacuum holding performance for over 2 months.

The programmable features of the camera system permit flexible camera configurations for single/multi read outs, programmable bias and clocks voltages and multi phase timing waveform generation. The host PC enables the development and down loading of DSP codes from a high-level language (Delphi). The data-acquisition software has been developed in Delphi operating under windows 95/98/NT. The object-oriented approach has simplified the application development and has built-in features to meet any change in hardware requirement. The software takes advantages of the objects in providing an

effective user interface, graphical display and data storage. The software developed for the mosaic camera could easily be tuned for testing other CCDs like STOO2AB and S1424, demonstrating its flexibility. A hardware lossless data compression scheme has been realized as part of this camera controller.

A few problems posed by the Thomson CCDs have been solved. (i) The first problem related to crosstalk. A crosstalk was noticed between various channels with the Thomson CCDs, when operated with common bias voltages for the readout sections. A cross coupling of about 3-4% was seen in the adjacent readout channels. Providing independent bias supplies for the readouts effectively eliminated the cross coupling. (ii) Two of the THX789M CCDs failed during our initial tests and trial observations. A high drain current caused by operating the VGMOS at the recommended value of 7.7V has caused the output amplifier failure. The drain current is programmable through the gate voltage VGMOS. This gate voltage is found to be very crucial. A safe operation was achieved by operating the gate at a reduced 7.0V. But this reduction in VGMOS reduced the CCD source follower gain causing higher noise.

7.2 Laboratory experiment and results

A laboratory arrangement was set up in order to calibrate the mosaic CCDs. The noise, gain, linearity and quantum efficiency measurements were carried out on the mosaic CCDs. A noise figure of about 18 electrons was obtained for the mosaic CCD camera system. The system non-linearities have been estimated to be 0.1 to 0.2 for three CCDs and 0.36 for the fourth CCD. The full-well capacity of each mosaic CCDs was measured to be around 220K electrons and this value closely agrees with the typical manufacturer specifications. The quantum efficiency measurements show that all the CCDs in mosaic have similar response. The laboratory characterization also indicated that one of the CCDs in the mosaic configuration (CCD-A) has a huge defect scanning over 1000 pixels in the middle of the imaging area. The charge shifting was affected at all signal levels subsequent to this defect in this CCD.

7.3 Observations and results from a Study of the cluster NGC 6631

In order to evaluate the mosaic camera performance, the system was used to observe the open cluster NGC 6631 at 1-m telescope, State Observatory, Nainital. This photometry results were compared with the results from the previous observations of the same cluster with the UPSO CCD camera system. The comparisons show that the observed magnitude differences are with in 0.1m for stars up to 18 mag. These differences are fairly random and show no systematic errors. The errors become more that 0.1 for the stars fainter than V = 18 mag. This appears to be mostly due to the fact that a few stars that were treated as single with the UPSO CCD observations resolved into double stars with the mosaic CCD system. Considering this and the uncertainties present in the photometric measurements, we conclude that the performance of the mosaic CCD camera system is satisfactory.

The open cluster NGC 6631 was observed in Johnson V and Cousins I passbands. These observations were calibrated by observing two standard fields. Each CCD in the mosaic was processed independently and its data was reduced using standard reduction techniques. A color magnitude diagram (V, V-I) was obtained down to 20 magnitude from the observations. Radial variation of the stellar surface density obtained from the data is used to estimate cluster radius and the field star contamination. The theoretical stellar evolutionary isochrones from Bertelli are used to estimate the cluster parameters. A metal-rich model for an age of 400 Myrs. fit the data reasonably well. The isochrones explained the presence of stars around the main sequence turn-off and some fraction of the cluster members seems to be in the form of binaries. The distance of the cluster is estimated to be around 2.6 + 0.5 kpc. The slope of the mass-function of the cluster is determined to be 2.1 + 0.5.

7.4 Suggestions on improvement to the present camera system

Some improvements to the existing hardware and software of the camera system have become feasible while concluding this thesis work. These improvements relate to a high speed read out, a fiber optic link for better noise-immunity, implementation of the host

interface on a PCI bus, a direct waveform editor and porting the application software to a Linux platform.

The analog signal processing board needs to be updated to achieve higher speeds. One can plan to implement a design that can support both the DCS and clamp sample signal processing techniques. Using a faster ADC can directly increase the pixel rate. Datel has a 16-bit sampling ADC (ADS-937) with a 1 micro second acquisition and conversion time. The small size of the ADC allows accommodating 4 analog signal processing chains in a single PCB. The digital glue logic can be implemented in gate arrays, which will result in improved reliability and compact size of the controller. Providing a high-speed fiber-optic data link between the host computer and the controller can improve the system noise immunity. The host interface can be made to work in a PCI bus environment to achieve high throughputs.

Automating the CCD calibration procedure reduces the time in calibrating the CCDs. An X-ray calibration facility will enable one to obtain the camera gain instantly without the need for time consuming photon transfer technique. The X-ray facility will also help in estimating the charge transfer efficiency. A user interactive waveform-editing tool will be useful by which one can directly generate the time and state fields to an output ASCII file. The data acquisition software can be ported into a Linux platform, which would provide compatible data to the reduction packages like IRAF, DAOPHOT, etc. The software developed with Delphi can be directly ported to Linux using the Kylix software.

List of publications

- A DSP Based Digital Pattern Generator for Charge Coupled Devices
  B. Nagaraja Naidu and R. Srinivasan, *Proc. of International Conference on Instrumentation-96*, 332-337, Aug 8-10, 96.

- Advances of Charge Coupled Devices in Electronic Imaging
  B. Nagaraja Naidu & R. Srinivasan, *IETE Technical Review*, Vol. 14, Nos. 4 & 5, 331-341, Jul-Oct. 97

- Development of CCD CameraSystem at IIA
  B. Nagaraja Naidu, S. Murali Shankar and R. Srinivasan, *Proc. of Silver Jubilee WorkShop on Astronomy with Moderate Size Telescope, Bull. of Astronomical Society of India*, (1998) 26, pp387-395.,

- Object Oriented Programming Approach to CCD Data Acquisition and Image Processing
  B. Nagaraja Naidu, R. Srinivasan and S. Murali Shankar, *Proc. of SPIE, Vol. 3114*, pp260-269, 1997

- A modular CCD cryostat for large format and mosaic CCDs
  B. Nagaraja Naidu, R. Srinivasan and K. Sagay Nathan, *Bull. Astr. Soc. Of India*, June, 2001.

- A DSP based mosaic CCD camera controller
  B. Nagaraja Naidu & R. Srinivasan, *Proceedings of the IEEE Electro/Information Technology Conference*, 7-9, June, 2001, Oakland University, Chicago.

- A Hardware Approach to Loss-less Data Compression
  B. Nagaraja Naidu and R. Srinivasan, *Proceedings of the IEEE Electro/Information Technology Conference*, 7-9, June, 2001, Oakland University, Chicago.

- Performance of the IIA Mosaic CCD Camera System
  B. Nagaraja Naidu, R. Srinivasan, V.Mohan, Ram Sagar, *Submitted to Bull. Astr. Soc. Of India*, Aug. 2001

- A deep VI CCD photometric study of the galactic star cluster NGC 6631
  Ram Sagar, B. Nagaraja Naidu and V. Mohan, *Submitted to Bull. Astr. Soc. Of India*, Aug. 2001

Appendix: A

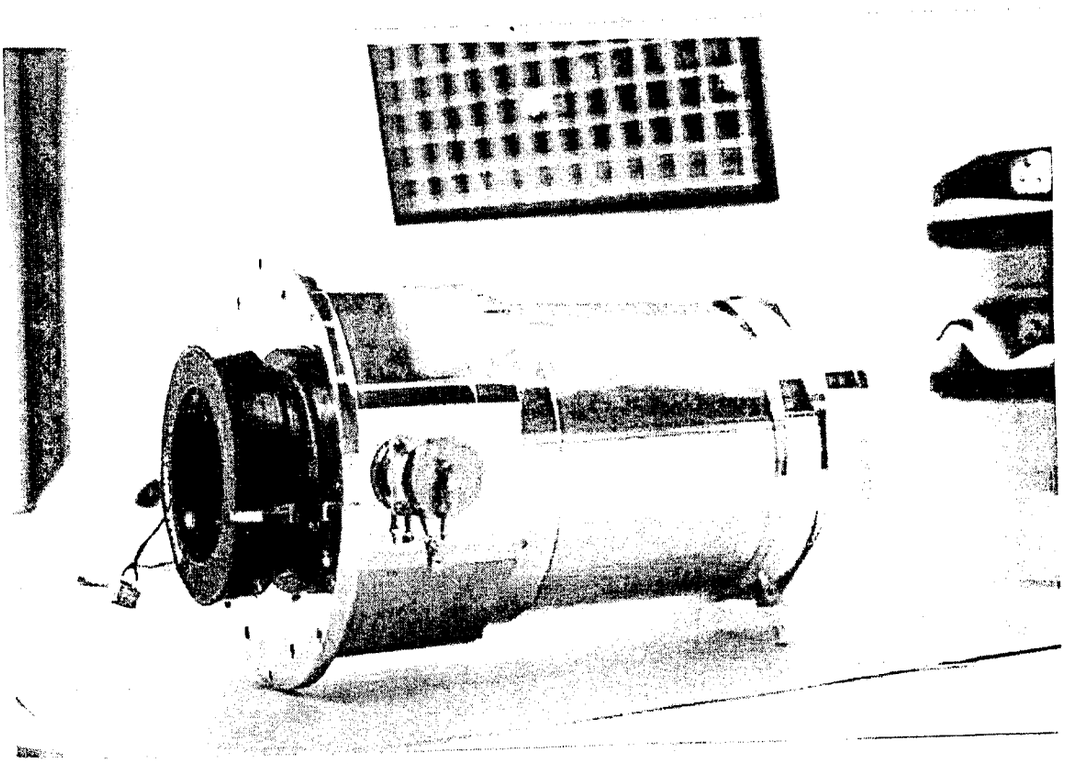


Photo 1: Modular IIA CCD cryostat

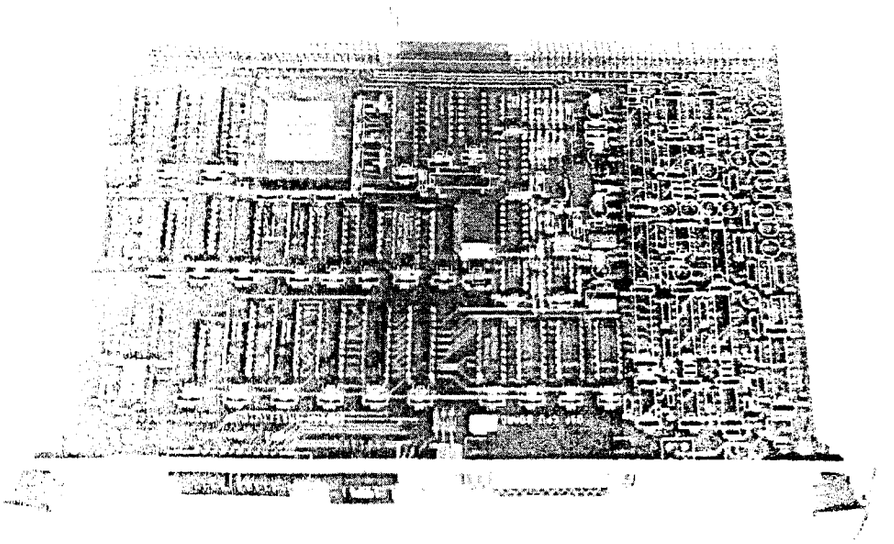


Photo 2: DSP CPU board

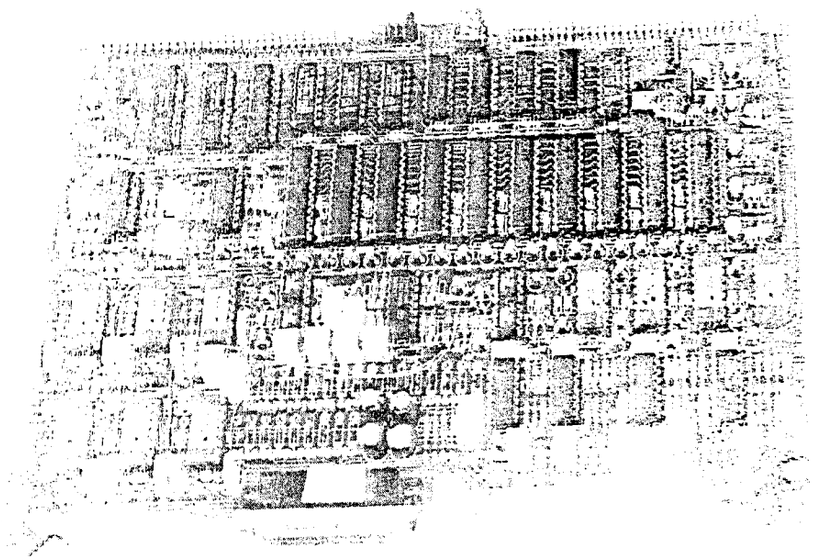


Photo 3: Bias and clocks board

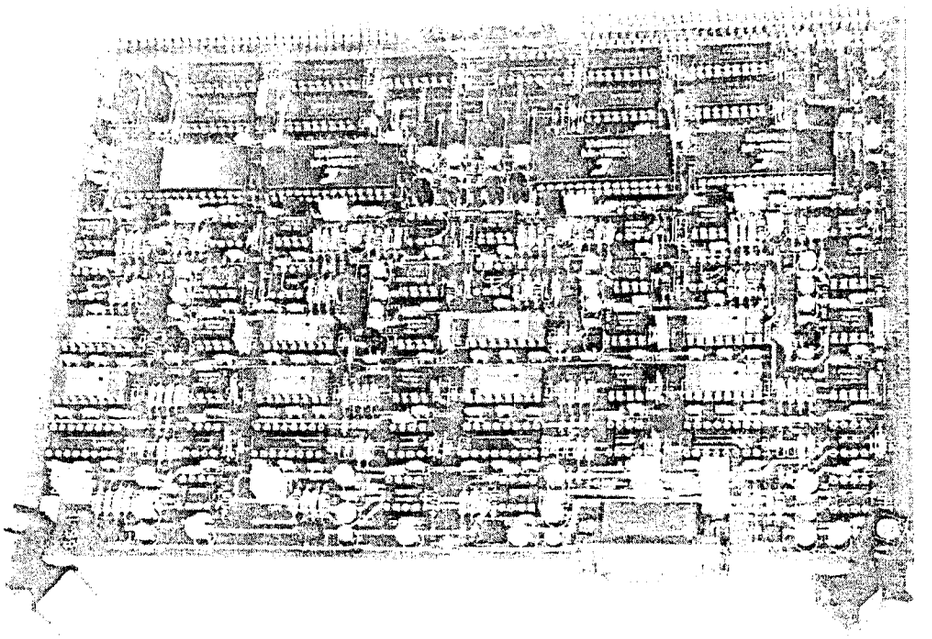


Photo 4: Signal processing board

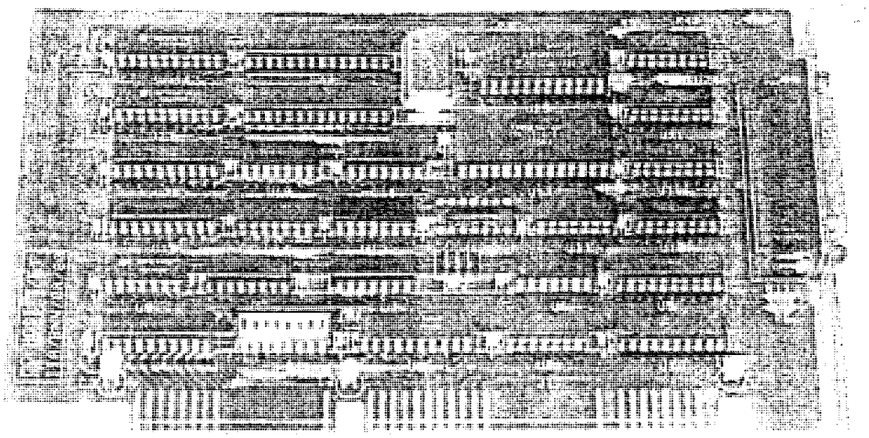


Photo 5: Host interface board

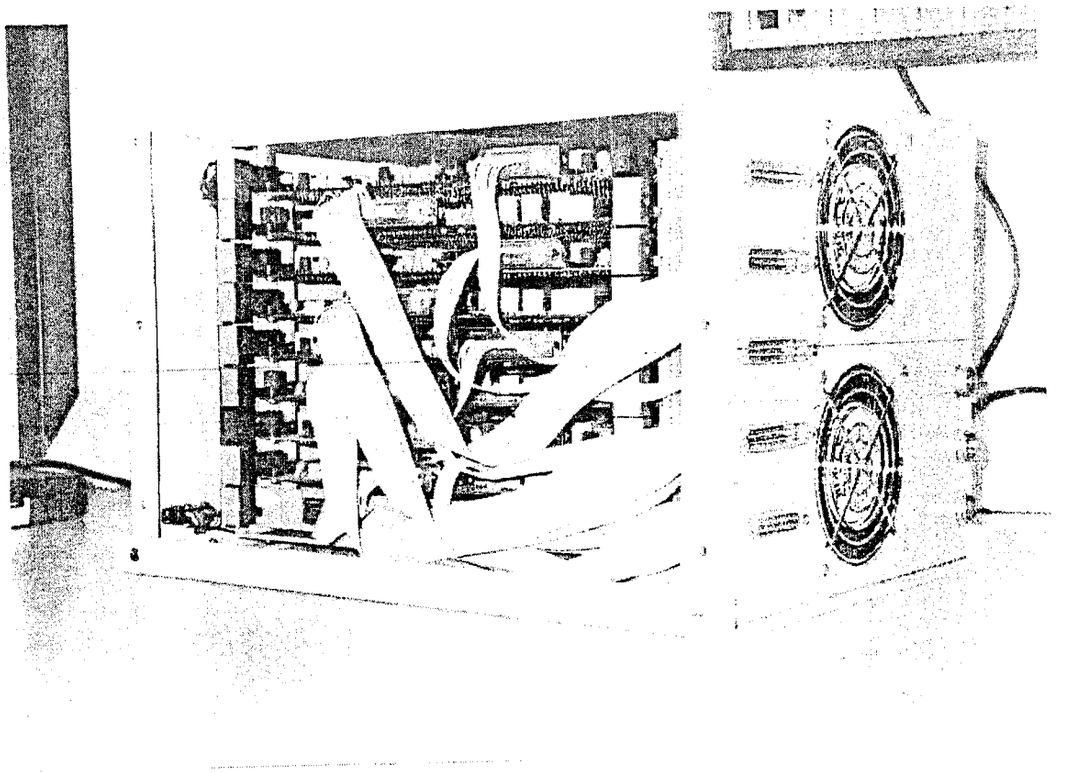


Photo 6: Mosaic CCD controller enclosure

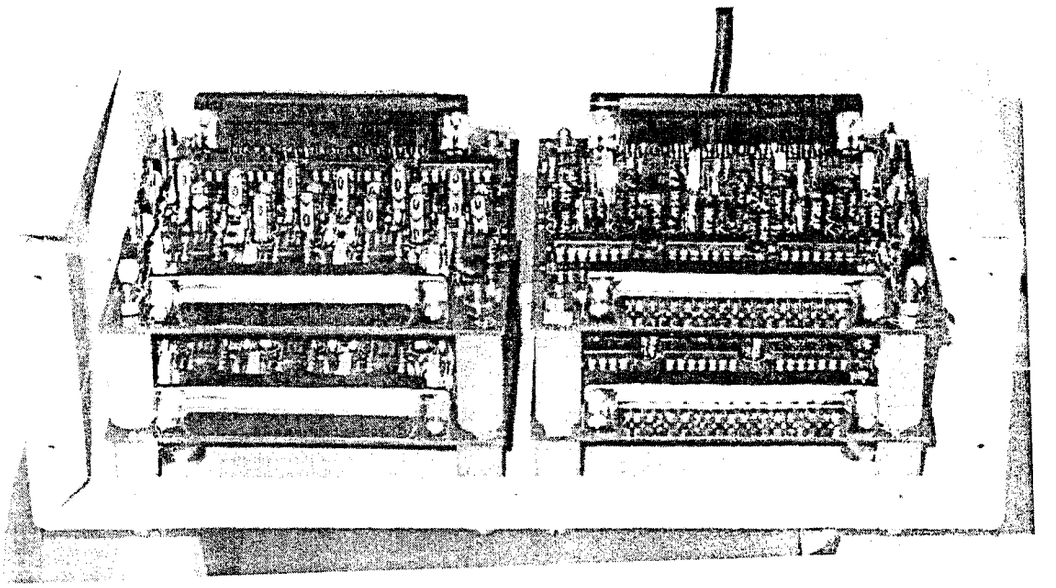


Photo 7: Bias buffers and pre-amplifier box

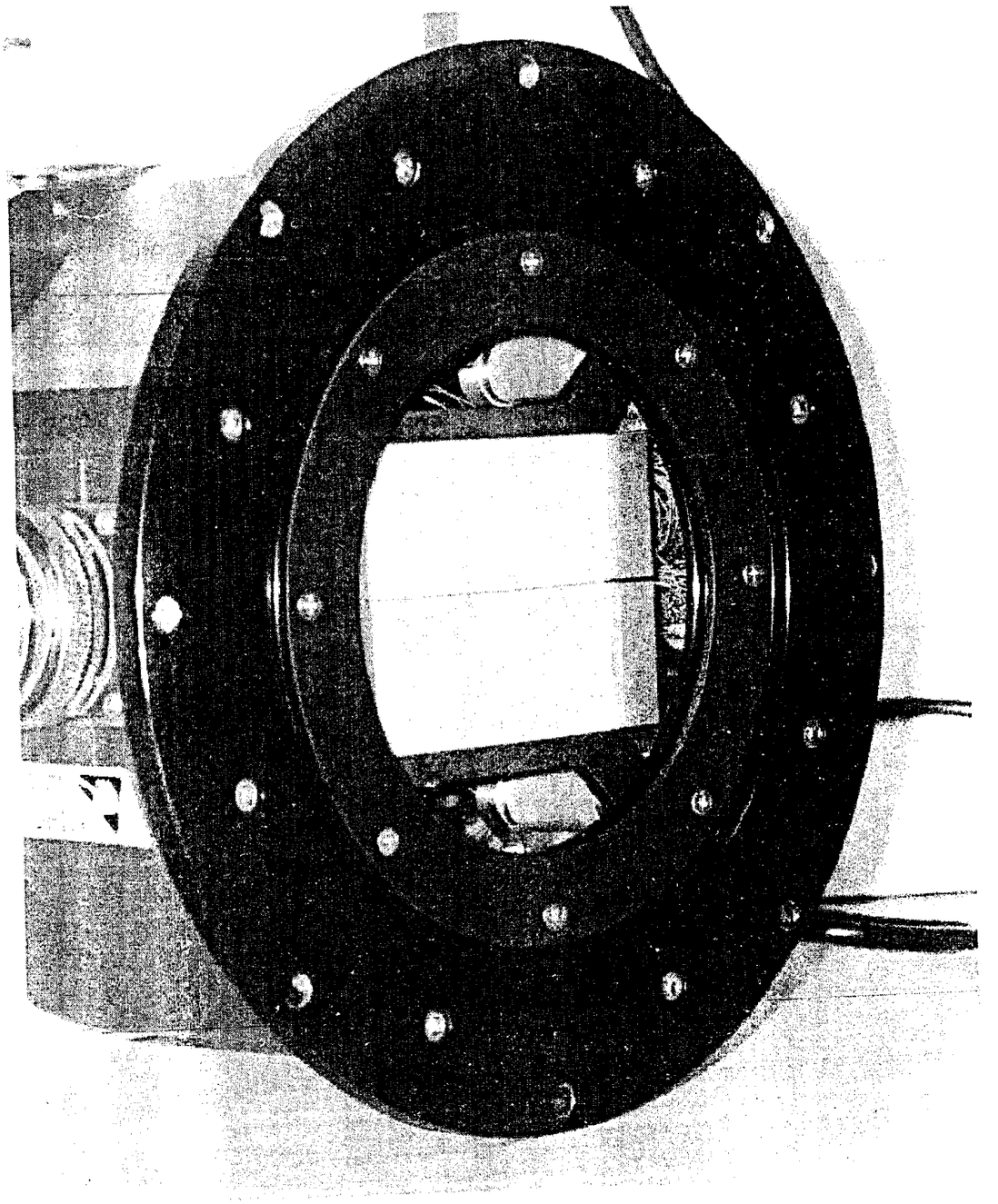


Photo 8: Mosaic CCD camera head view

Appendix: B

DSP ASSEMBLY CODE

```
;       DSP 56000, ASM56000 assembler program to control mosaic ccd
;       Date 26/03/99
;       Naidu

START   EQU     $0040           ;Start of program
PCC     EQU     $FFE1           ;PortC control reg
SCR     EQU     $FFF0           ;SCI control reg
SCCR    EQU     $FFF2           ;SCI clock control reg
SSR     EQU     $FFF1           ;SCI status reg
SRXL    EQU     $FFF4           ;SCI receive reg. low byte
STXL    EQU     $FFF4
PBC     EQU     $FFE0           ;PortB control reg
PBDDR   EQU     $FFE2           ;PortB data direction deg
PBD     EQU     $FFE4           ;PortB data reg
LATCH   EQU     $FFC0           ;Latch address for X Y
                                  dataspace
TCSR    EQU     $FFDE           ;Timer counter status register
ADCBASE EQU     $3600           ;ADC base addr for board1
OUTECHO EQU     $0200           ;Echo byte output latch address
INECHO  EQU     $0300           ;Echo byte input latch address


        ORG     P:START         ;Start
        ORI     #$03,MR

        MOVEP   #$0,X:PBC       ;Port-B as GP I/O
        MOVEP   #$00FF,X:PBDDR
        MOVEP   #$0,X:PBD
        MOVE    #$3600,X0       ;Base Address Sinal processing
        MOVE    X0,X:$00        ;board # 1
        MOVE    #$5600,X0
        MOVE    X0,X:$01        ;board # 2
        MOVE    #$7600,X0
        MOVE    X0,X:$02        ;board # 3
        MOVE    #$9600,X0
        MOVE    X0,X:$03        ;board # 4

        MOVEP   #$0140,X:TCSR   ;TIO as GPIO
        BSET    #10,X:TCSR      ;Set TIO high

        MOVEP   #$0302,X:SCR    ;Disable TX, RX interrupts
                                ;Enable TX  RX  8bit Async
                                ;(1 Start, 8 data  1 stop
        MOVEP   #$C000,X:SCCR   ;External TX  RX at PCLK
        MOVEP   #$07,X:PCC      ;Select SCI  TX and R, PC2 I/O


        DO      #3,LOOP1
HERE    JCLR    #2,X:SSR,SELF   ;Wait for RDRF to get high
SELF    MOVEP   X:SRXL,A2       ;Put 8 bits  A2
        REP     #8
        ASR     A

LOOP1   JSSET   #16,A1,LOADDAC  ;Sub routine
        JSSET   #17,A1,OUTDATA
        JSSET   #18,A1,PARALLEL
```

```
                JSSET   #19,A1,SERIAL
                JSSET   #20,A1,SHIFT
                JSSET   #21,A1,PREFLUSH
                MOVEP   #$AA,X:STXL     ;Echo the Execution of command
                JSSET   #22,A1,READROW
                JSSET   #23,A1,RESET
                JMP     HERE

LOADDAC         MOVEP   #$0,X:PBD       ;Load selected DAC with data
                MOVE    #$E000,X1
                MOVEP   A1,Y:$FFC0
                OR      X1,A
                REP     #10
                NOP
                MOVEP   A1,Y:$FFC0
                RTS

OUTDATA         MOVEP   #$0,X:PBD       ;Output data on back plane
                MOVEP   A1,Y:$FFC0
                RTS

PARALLEL        MOVEP   #$1F,X:PBD      ;Parallel waveform generation
                MOVEP   #$C8D3C8,Y:LATCH
                MOVEP   #$C8D3C8,Y:LATCH
                MOVEP   #$C8D3D8,Y:LATCH
                MOVEP   #$C8D3DB,Y:LATCH
                MOVEP   #$C8D3D3,Y:LATCH
                MOVEP   #$C8D3D7,Y:LATCH
                MOVEP   #$C8D3C7,Y:LATCH
                MOVEP   #$C8D3CF,Y:LATCH
                MOVEP   #$50D3CF,Y:LATCH
                MOVEP   #$78D3CC,Y:LATCH
                MOVEP   #$C8D3C8,Y:LATCH
                MOVEP   #$C8D3C0,Y:LATCH
                RTS

PREFLUSH        MOVEP   #$1F,X:PBD      ;Preflush waveform generation
                DO      #100,PFLOOP
                DO      #21,PBIN
                JSR     PARALLEL
                NOP
PBIN            NOP
                JSR     SHIFT
                NOP
PFLOOP          NOP
                RTS

SERIAL          MOVEP   #$1F,X:PBD      ;Serial waveform generation
                MOVEP   #$325380,Y:LATCH
                MOVEP   #$3253A0,Y:LATCH
                MOVEP   #$325320,Y:LATCH
                MOVEP   #$325360,Y:LATCH
                MOVEP   #$325260,Y:LATCH
                MOVEP   #$3252E0,Y:LATCH
                MOVEP   #$3252C0,Y:LATCH
                MOVEP   #$C853C0,Y:LATCH
                MOVEP   #$C853C0,Y:LATCH
                MOVEP   #$6457C0,Y:LATCH
                MOVEP   #$C853C0,Y:LATCH
                MOVEP   #$C853C0,Y:LATCH
                MOVEP   #$6463C0,Y:LATCH
```

```
                MOVEP   #$6463C0,Y:LATCH
                MOVEP   #$647180,Y:LATCH
                MOVEP   #$647980,Y:LATCH
                MOVEP   #$C87980,Y:LATCH
                MOVEP   #$C87980,Y:LATCH
                MOVEP   #$646980,Y:LATCH
                MOVEP   #$646980,Y:LATCH
                MOVEP   #$643980,Y:LATCH
                MOVEP   #$645980,Y:LATCH
                MOVEP   #$645980,Y:LATCH
                MOVEP   #$645980,Y:LATCH
                MOVEP   #$01,X:PBD
                RTS

SHIFT           DO      #522,SHIFTLOOP   ;Serial shift without DCS
                MOVEP   #$1F,X:PBD
                MOVEP   #$646380,Y:LATCH
                MOVEP   #$6463A0,Y:LATCH
                MOVEP   #$647120,Y:LATCH
                MOVEP   #$646960,Y:LATCH
                MOVEP   #$646860,Y:LATCH
                MOVEP   #$641EE0,Y:LATCH
                MOVEP   #$645EC0,Y:LATCH
                MOVEP   #$645BC0,Y:LATCH
SHIFTLOOP       NOP
                RTS

STRBDATA        MOVEP   #$0,X:PBD        ;Strobe data of all channels
                MOVE    #$00,R0
                DO      #4,ALLFOUR
                MOVE    X:(R0)+,B0
                DO      #4,ADCDATA
                MOVEP   B0,Y:LATCH
                NOP
                BCLR    #10,X:TCSR
                NOP
                BSET    #10,X:TCSR
                INC     B
                NOP
                MOVEP   B0,Y:LATCH
                NOP
                BCLR    #10,X:TCSR
                NOP
                BSET    #10,X:TCSR
                INC     B
ADCDATA         NOP
                NOP
ALLFOUR         NOP
                MOVEP   #$01,X:PBD
                ;MOVEP   #$5380,Y:LATCH
                MOVEP   #$5980,Y:LATCH
                RTS

READROW         BCLR    #22,A1          ;Shift no. of rows (A1)
                DO      A1,NOOFROWS
                JSR     PARALLEL
                DO      #9,PRESCAN
                JSR     SERIAL
                NOP
PRESCAN         NOP
                DO      #512,HSHIFT
```

```
                JSR     SERIAL
                JSR     STRBDATA
                NOP
HSHIFT          NOP
                NOP
NOOFROWS        NOP
                RTS

RESET           MOVEP   #0,X:$FFFF     ;Software reset
                MOVEC   #$12,OMR
                NOP
                JMP     <$0
                RTS

                END
```

LOAD (*.LOD) FILE

```
_START TIMING6M 0000 0000 0000 DSP56000 5.3.2

_DATA P 0040
0003F8 08F4A0 000000 08F4A2 0000FF 08F4A4 000000 44F400
003600 440000 44F400 005600 440100 44F400 007600 440200
44F400 009600 440300 08F49E 000140 0A9E2A 08F4B0 000302
08F4B2 00C000 08F4A1 000007 060380 000062 0AB182 00005E
084A34 0608A0 200022 0BCC30 000076 0BCC31 000080 0BCC32
000084 0BCC33 0000AD 0BCC34 0000E2 0BCC35 00009F 08F4B4
0000AA 0BCC36 000138 0BCC37 00014A 0C005C 08F4A4 000000
45F400 00E000 09CC00 200062 060AA0 000000 09CC00 00000C
08F4A4 000000 09CC00 00000C 08F4A4 00001F 09F480 C8D3C8
09F480 C8D3C8 09F480 C8D3D8 09F480 C8D3DB 09F480 C8D3D3
09F480 C8D3D7 09F480 C8D3C7 09F480 C8D3CF 09F480 50D3CF
09F480 78D3CC 09F480 C8D3C8 09F480 C8D3C0 00000C 08F4A4
00001F 066480 0000AA 061580 0000A6 0D0084 000000 000000
0BF080 0000E2 000000 000000 00000C 08F4A4 00001F 09F480
325380 09F480 3253A0 09F480 325320 09F480 325360 09F480
325260 09F480 3252E0 09F480 3252C0 09F480 C853C0 09F480
C853C0 09F480 6457C0 09F480 C853C0 09F480 C853C0 09F480
6463C0 09F480 6463C0 09F480 647180 09F480 647980 09F480
C87980 09F480 C87980 09F480 646980 09F480 646980 09F480
643980 09F480 645980 09F480 645980 09F480 645980 08F4A4
000001 00000C 060A82 0000F5 08F4A4 00001F 09F480 646380
09F480 6463A0 09F480 647120 09F480 646960 09F480 646860
09F480 641EE0 09F480 645EC0 09F480 645BC0 000000 00000C
08F4A4 000000 300000 060480 00010E 51D800 060480 00010C
09C900 000000 0A9E0A 000000 0A9E2A 000009 000000 09C900
000000 0A9E0A 000000 0A9E2A 000009 000000 000000 000000
08F4A4 000001 09F480 005980 00000C 08F4A4 000000 060480
000135 212D00 0ACD48 44F400 000200 20004A 09CD00 45F400
00E000 20006A 09CD00 09F480 000300 0A9E0A 000000 000000
0A9E2A 000000 000000 09F480 000200 09F480 00E000 09F480
000300 0A9E0A 000000 000000 0A9E2A 000000 000000 00000C
0ACC56 06CC00 000147 0D0084 060980 00013F 0D00AD 000000
000000 060082 000145 0D00AD 0D00F8 000000 000000 000000
000000 00000C 08F4BF 000000 0512BA 000000 0C0000 00000C
_SYMBOL P
HERE                    I 00005C
SELF                    I 00005E
LOOP1                   I 000063
LOADDAC                 I 000076
OUTDATA                 I 000080
PARALLEL                I 000084
PREFLUSH                I 00009F
PBIN                    I 0000A7
PFLOOP                  I 0000AB
SERIAL                  I 0000AD
SHIFT                   I 0000E2
SHIFTLOOP               I 0000F6
STRBDATA                I 0000F8
ADCDATA                 I 00010D
ALLFOUR                 I 00010F
SENDDATA                I 000115
SENDEND                 I 000136
READROW                 I 000138
PRESCAN                 I 000140
HSHIFT                  I 000146
NOOFROWS                I 000148
```

```
RESET                   I 00014A
_SYMBOL N
START                   I 000040
PCC                     I 00FFE1
SCR                     I 00FFF0
SCCR                    I 00FFF2
SSR                     I 00FFF1
SRXL                    I 00FFF4
STXL                    I 00FFF4
PBC                     I 00FFE0
PBDDR                   I 00FFE2
PBD                     I 00FFE4
LATCH                   I 00FFC0
TCSR                    I 00FFDE
ADCBASE                 I 003600
OUTECHO                 I 000200
INECHO                  I 000300

_END 0040
```

BOOTSTRAP CODE

```
;No of program words, start address.
100100 400000
;Program memory location followed by 8 program words in each line
0000  000000  000000  000000  000000  000000  000000  000000  000000
0008  000000  000000  000000  000000  000000  000000  000000  000000
0010  000000  000000  000000  000000  000000  000000  000000  000000
0018  000000  000000  000000  000000  000000  000000  000000  000000
0020  000000  000000  000000  000000  000000  000000  000000  000000
0028  000000  000000  000000  000000  000000  000000  000000  000000
0030  000000  000000  000000  000000  000000  000000  000000  000000
0038  000000  000000  000000  000000  000000  000000  000000  000000
0040  0003F8  08F4A0  000000  08F4A2  0000FF  08F4A4  000000  44F400
0048  003600  440000  44F400  005600  440100  44F400  007600  440200
0050  44F400  009600  440300  08F49E  000140  0A9E2A  08F4B0  000302
0058  08F4B2  00C000  08F4A1  000007  060380  000062  0AB182  00005E
0060  084A34  0608A0  200022  0BCC30  000076  0BCC31  000080  0BCC32
0068  000084  0BCC33  0000AD  0BCC34  0000E2  0BCC35  00009F  08F4B4
0070  0000AA  0BCC36  000138  0BCC37  00014A  0C005C  08F4A4  000000
0078  45F400  00E000  09CC00  200062  060AA0  000000  09CC00  00000C
0080  08F4A4  000000  09CC00  00000C  08F4A4  00001F  09F480  C8D3C8
0088  09F480  C8D3C8  09F480  C8D3D8  09F480  C8D3DB  09F480  C8D3D3
0090  09F480  C8D3D7  09F480  C8D3C7  09F480  C8D3CF  09F480  50D3CF
0098  09F480  78D3CC  09F480  C8D3C8  09F480  C8D3C0  00000C  08F4A4
00A0  00001F  066480  0000AA  061580  0000A6  0D0084  000000  000000
00A8  0BF080  0000E2  000000  000000  00000C  08F4A4  00001F  09F480
00B0  325380  09F480  3253A0  09F480  325320  09F480  325360  09F480
00B8  325260  09F480  3252E0  09F480  3252C0  09F480  C853C0  09F480
00C0  C853C0  09F480  6457C0  09F480  C853C0  09F480  C853C0  09F480
00C8  6463C0  09F480  6463C0  09F480  647180  09F480  647980  09F480
00D0  C87980  09F480  C87980  09F480  646980  09F480  646980  09F480
00D8  643980  09F480  645980  09F480  645980  09F480  645980  08F4A4
00E0  000001  00000C  060A82  0000F5  08F4A4  00001F  09F480  646380
00E8  09F480  6463A0  09F480  647120  09F480  646960  09F480  646860
00F0  09F480  641EE0  09F480  645EC0  09F480  645BC0  000000  00000C
00F8  08F4A4  000000  300000  060480  00010E  51D800  060480  00010C
0100  09C900  000000  0A9E0A  000000  0A9E2A  000009  000000  09C900
0108  000000  0A9E0A  000000  0A9E2A  000009  000000  000000  000000
0110  08F4A4  000001  09F480  005980  00000C  08F4A4  000000  060480
0118  000135  212D00  0ACD48  44F400  000200  20004A  09CD00  45F400
0120  00E000  20006A  09CD00  09F480  000300  0A9E0A  000000  000000
0128  0A9E2A  000000  000000  09F480  000200  09F480  00E000  09F480
0130  000300  0A9E0A  000000  000000  0A9E2A  000000  000000  00000C
0138  0ACC56  06CC00  000147  0D0084  060980  00013F  0D00AD  000000
0140  000000  060082  000145  0D00AD  0D00F8  000000  000000  000000
0148  000000  00000C  08F4BF  000000  0512BA  000000  0C0000  00000C
0150  000000  000000  000000  000000  000000  000000  000000  000000
  .     .       .       .       .       .       .       .       .
  .     .       .       .       .       .       .       .       .
01F0  000000  000000  000000  000000  000000  000000  000000  000000
01F8  000000  000000  000000  000000  000000  000000 000000 000000
```

Appendix: C

Memory Pointers for Single CCD Readout

```
procedure TMCUnitForm.ReadFullFrame(var ptrdata: pointer;
                                    var width, height: integer);
var
  DataAddr, StatusAddr, i, j, k, data, tempdata: word;
  ptrdatainit, ptrdata1, ptrdata1init: pointer;
  AData: longint;
begin
  ptrdatainit:= ptrdata;
  ptrdata1:= ptrdata;
  DataAddr:= ba + 2;
  StatusAddr:= ba + 4;
  AData:= $40000A; {flush first 10 rows}
  SendAData(AData);
  delay(500);
  if (ConfigForm.SelectMemory = 'AorB') then
    inc(longint(ptrdata1), 2047*2);
  if (ConfigForm.SelectMemory = 'CorD') then
    inc(longint(ptrdata1), 2048*2048*2 - 2048*2);
  ptrdata1init:= ptrdata1;
  ResetFIFOs;
  AData:= $400806; {do for 2048 rows}
  SendAData(AData);
  asm cli end;
  for j:= 1 to height do
  begin
    while (port[ba+4] and 8) = 8 do ;
    for i:= 1 to width div 4 do begin
      for k:= 1 to 4 do begin
        word(ptrdata1^):= swap(portw[ba+2]);
        if (ConfigForm.SelectMemory = 'AorB') then
          dec(longint(ptrdata1),1024);
        if (ConfigForm.SelectMemory = 'CorD') then
          inc(longint(ptrdata1),1024);
      end;
      ptrdata1:= ptrdata1init;
      if (ConfigForm.SelectMemory = 'AorB') then
        dec(longint(ptrdata1), i*2);
      if (ConfigForm.SelectMemory = 'CorD') then
        inc(longint(ptrdata1), i*2);
    end;
    if (ConfigForm.SelectMemory = 'AorB') then
      inc(longint(ptrdata1init), 2048*2);
    if (ConfigForm.SelectMemory = 'CorD') then
      dec(longint(ptrdata1init), 2048*2);
    ptrdata1:= ptrdata1init;
  Form1.StatusBar.Panels[2].Text:= inttostr(j);
  end;
  asm sti end;
  ptrdata:= ptrdatainit; ptrdata1:= ptrdata;
  ptrdata1init:= ptrdata;
end;
```

Memory Pointers for mosaic CCD Readout

```
procedure TMCUnitForm.ReadMosaicFrame(var ptrdata: pointer;
                                      var width, height: integer);
  var
    DataAddr, StatusAddr, i, k, l: word;
    ptrdatainit, ptrdata1, ptrdata2: pointer;
    ptrdata1init, ptrdata2init: pointer;
    AData, j: longint;
  begin
    ptrdatainit:= ptrdata;
    DataAddr:= ba + 2;
    StatusAddr:= ba + 4;
    AData:= $40000A; {flush first 10 rows}
    SendAData(AData);
    delay(2000);
    inc(longint(ptrdata),(width-1)*2);
    ptrdata1:= ptrdata; ptrdata1init:= ptrdata1;
    ptrdata:= ptrdatainit;
    inc(longint(ptrdata),(width*height*2 - width*2));
    ptrdata2:= ptrdata; ptrdata2init:= ptrdata;
    ptrdata:= ptrdatainit;
    ResetFIFOs;
    AData:= $400806; {do for 2048 rows}
    SendAData(AData);
    for j:= 1 to 2048 do
    begin
      while (port[ba+4] and 8) = 8 do ;
      for i:= 1 to 256 do
      begin
        l:= i;
        for k:= 1 to 8 do
        begin
          word(ptrdata1^):= swap(portw[ba+2]);{swap(j);}
          dec(longint(ptrdata1),1024);
          if k= 4 then dec(longint(ptrdata1), ConfigForm.ColGap*2);
        end;
        for k:= 1 to 8 do
        begin
          word(ptrdata2^):= swap(portw[ba+2]);{swap(j);}
          inc(longint(ptrdata2),1024);
          if k= 4 then inc(longint(ptrdata2), ConfigForm.ColGap*2);
        end;
        ptrdata1:= ptrdata1init;
        dec(longint(ptrdata1), i*2);
        ptrdata2:= ptrdata2init;
        inc(longint(ptrdata2), i*2);
      end;

      while (port[ba+4] and 8) = 8 do ;
      for i:= 257 to 512 do
      begin
        l:= i;
        for k:= 1 to 8 do
        begin
          word(ptrdata1^):= swap(portw[ba+2]);{swap(j);}
          dec(longint(ptrdata1),1024);
          if k= 4 then dec(longint(ptrdata1), ConfigForm.ColGap*2);
        end;
        for k:= 1 to 8 do
        begin
```

```
        word(ptrdata2^):= swap(portw[ba+2]);{swap(j);}
        inc(longint(ptrdata2),1024);
        if k= 4 then inc(longint(ptrdata2), ConfigForm.ColGap*2);
      end;
      ptrdata1:= ptrdata1init;
      dec(longint(ptrdata1), i*2);
      ptrdata2:= ptrdata2init;
      inc(longint(ptrdata2), i*2);
    end;
    Form1.StatusBar.Panels[2].Text:= inttostr(j);
    inc(longint(ptrdata1init), width*2);
    dec(longint(ptrdata2init), width*2);
    ptrdata1:= ptrdata1init;
    ptrdata2:= ptrdata2init;
  end;
  ptrdata:= ptrdatainit; ptrdata1init:= ptrdata;
  ptrdata2init:= ptrdata; ptrdata1:= ptrdata; ptrdata2:= ptrdata;
  {AData:= $040000;
  SendAData(AData);}
end;
```

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